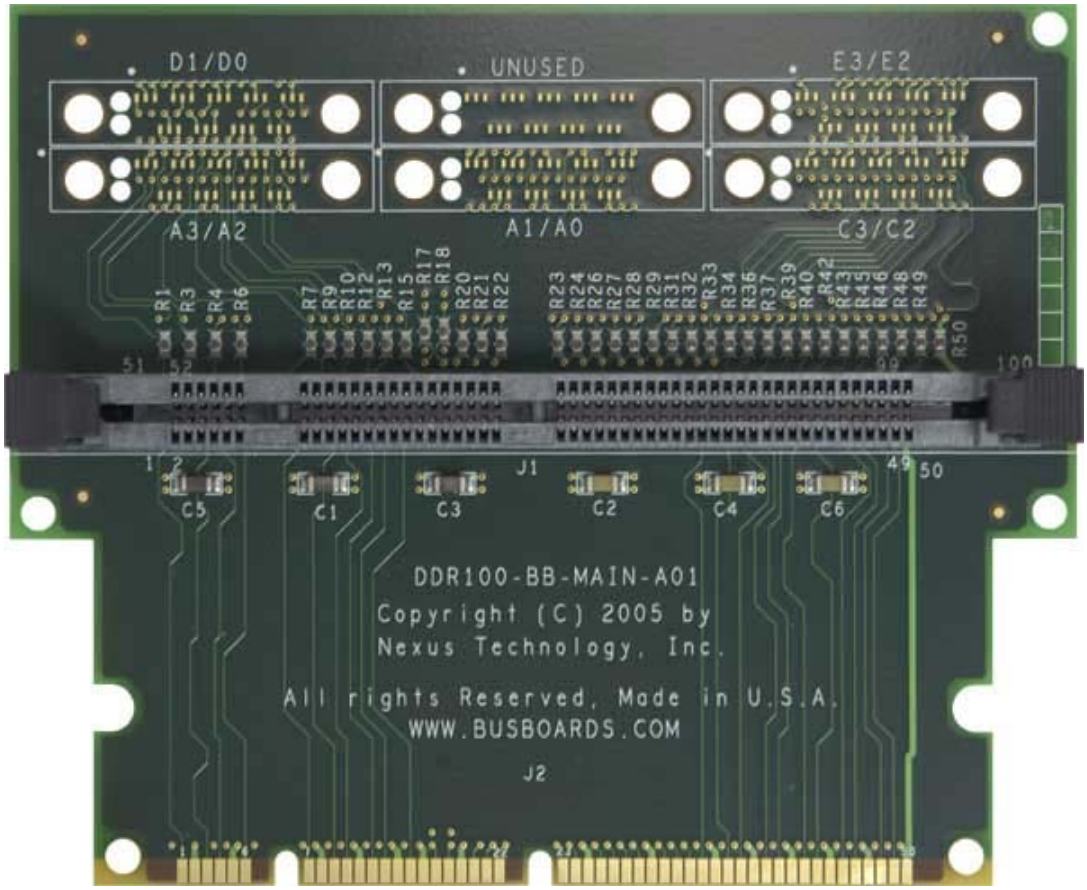
NEXUS TECHNOLOGY

100-pin, 2.5V Double Data Rate (DDR) Bus Analysis Probe & Software

NEX-DDR100P



- Quick and easy connection between the DDR bus and a Tektronix Logic Analyzer
- P6860 probe points available on either side of the adapter
- Extender design does not require a dedicated slot
- Supports 100-pin, 2.5V PC2100/PC2700, 32-bit wide Unbuffered or Registered DDR
- Impedance controlled
- Matched trace lengths
- No active buffering of the DDR signals
- Accurate 8GHz timing analysis
- Simultaneous state and timing on every channel of the TLA
- Trigger on setup/hold violations
- Correlation with data from other acquisition modules
- Use the TLA's Extended iView capabilities to view any channel on an oscilloscope without re-probing

General Description

The NEX-DDR100P adapter is designed to provide quick and easy connections to interface a TLA700 Logic Analyzer to a 100-pin, 2.5Volt PC2100/PC2700, 32-bit wide Unbuffered or Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Module (DDR SDRAM DIMM) socket. Connections are made through P6860 High-Density, Connectorless probes. Probe connection points are available on either side of the adapter. The ability to probe on either side of the adapter allows for flexible mechanical clearance and also provides the mechanical clearance necessary to allow two DDR sockets to be monitored simultaneously in a single target.

8Ghz Timing Analysis available for all DDR signals

Oscilloscope Connectivity on any channel without re-probing via the TLA's Enhanced iView Analog Mux capability.

No Dedicated Slot Required – The logic analyzer connects above the normal DIMM height so that there is no interference with adjacent DIMMs.

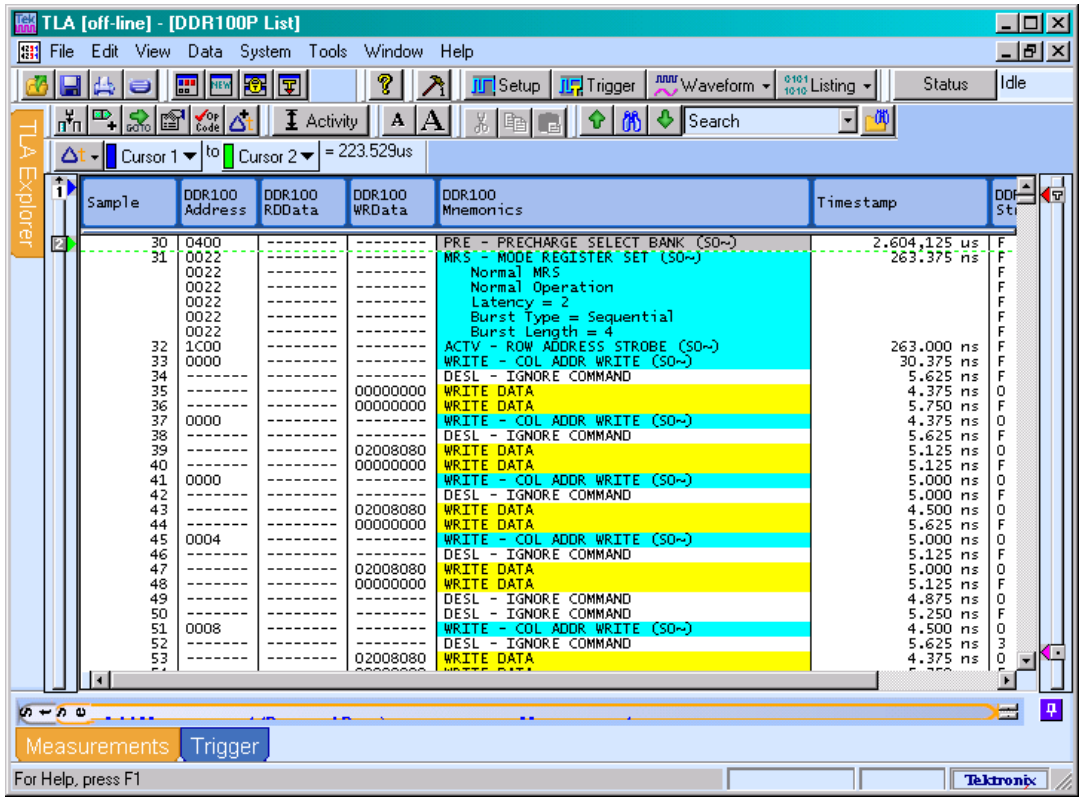
Symbol Disassembly Command types (Read, Write, Refresh, Precharge, Burst, NOP, Mode Register Set, etc.) are identified for quick analysis of bus activity

Correlating Bus Activity While the NEX-DDR100P package is being used to monitor the DDR bus activity, another acquisition module can be used to monitor activity elsewhere in the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred.

Logic Analyzer Configuration

DDR100 offers the ability to synchronously acquire up to 450Mhz data rate DDR Address and Command signals on every edge of the DDR Clock. Read Data and Write Data can also be acquired - the acquisition of DDR Data requires a valid data window of approximately 625ps. This support requires one TLA7Ax4 (136-channel) acquisition card with the 450MHz state clocking option and 4 P6860 probes. The DDR100 support is usable with a TLA7XX-series Logic Analyzer only, and the TLA must be running V4.2 or later of the TLA Application Software.

State Display



Ordering / Contact Information

Part Number NEX-DDR100P
Includes NEX-DDR100P adapter
DDR100 Support Software
Manual

Options include
NEX-DDRSPA - TLA Software Plug-In for determining optimum Setup & Hold sample points.

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

