DDR3 DIMM Slot Protocol Interposer

Flexible Protocol Validation

- Low cost visibility
- High speed DDR3 protocol validation
- Passive 240-pin DIMM slot interposer
- Designed for DDR3-2133+
- Automated Logic Analyzer Setup
- Full DDR3 Compliance Analysis
- Compatible with Nexus MA4100 Series Memory Analyzer
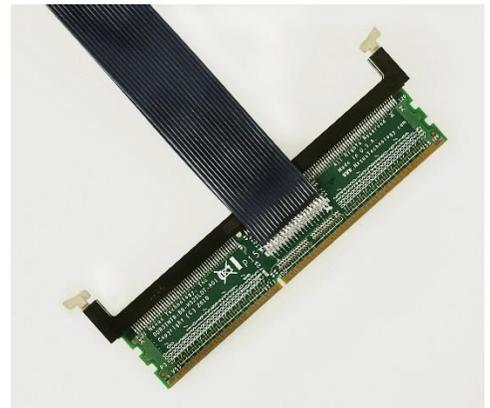
Overview

This interposer provides low cost monitoring of a DDR3 DIMM slot. Command, address and control information is shown is a display window for easy viewing. Protocol violation analysis software is included.

Performance You Can See™
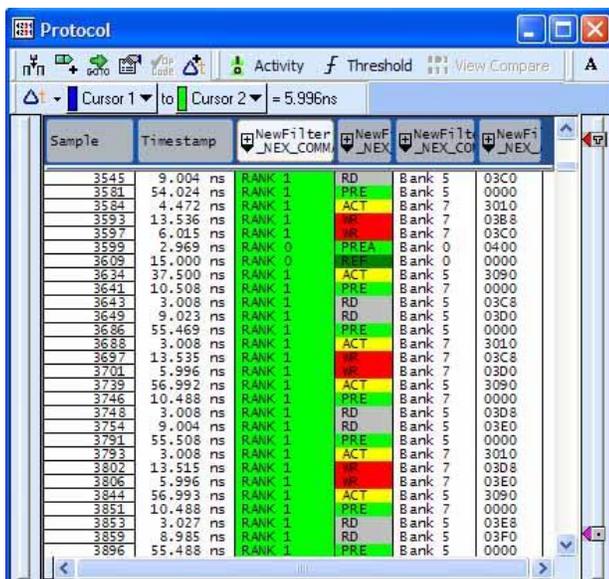
Figure 1 State Display of Command, Address, & Control
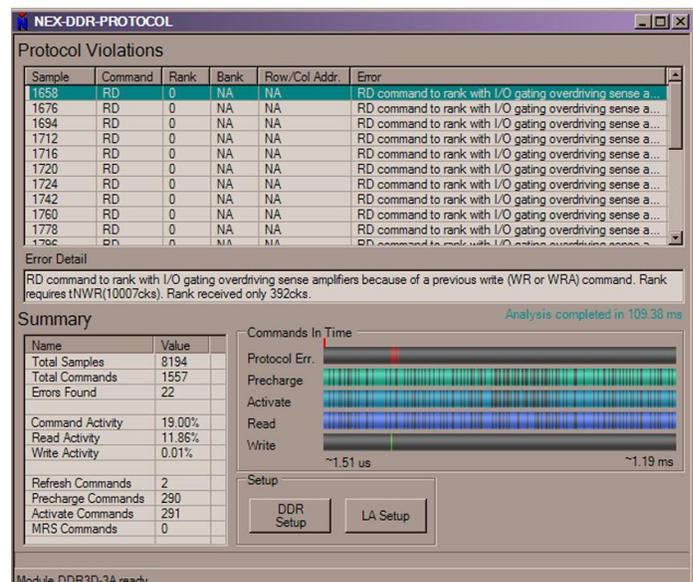

Figure 2 Protocol Violation Analysis

Software

This DDR3 DIMM slot protocol interposer comes with logic analyzer setup software that acquires and displays command, address, and control information from a DIMM slot. Protocol violation analysis software is also included.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions (Command, Address and Control only) for easy display and logic analyzer triggering/filtering.

Compliance Analysis Software
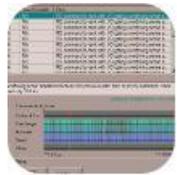
 There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the NEX-MCATLA-DDR3-SWL product webpage for more information.

Digital Validation

Logic analyzer setup software (TLA support package) is included with this product.

 The Optional Memory Compliance Analysis software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs protocol violation checking.

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NEX-DDR3INTR-P Technical Specification

General

Specification	Detail
Interface Type	Passive Interposer
LA Interface	NEX-PRB1-XL
JEDEC Module Type	DDR3 SDRAM Unbuffered or Registered DIMM
DDR3 Data Rates Supported (MT/s)	DDR3-2133+
Min. Voltage Swing	200mV
Min. Eye Width	200ps

Tektronix Hardware

Specification	Detail	Quantity
Logic Analyzer Mainframe	TLA7000	1
Logic Analyzer Module(s)	TLA7BB2/3/4 (1.4GHz Opt. Required for DDR3- >1333)	1
Logic Analyzer Probes	NEX-PRB1-XL	1

DDR3 Signals Probed

Specification	Detail
Command	RAS#, CAS#, WE#, CKE0, CKE1, RESET#, ODT0, ODT1
Addressing	CS0#, CS1#, CS2#, CS3#, A00-A15, BA0-BA2

Product Configurations

Nomenclature	LA Probes Included	Nexus Hardware Included	Nexus Software Included
NEX-DDR3INTR-P	No	1- DDR3 DIMM Slot Protocol Interposer	TLA Setup, Protocol Decode, and Protocol Violation Analysis
NEX-DDR3INTR-P-PR	Yes	1- DDR3 DIMM Slot Protocol Interposer 1- NEX-PRB1XL	TLA Setup, Protocol Decode, and Protocol Violation Analysis

Further Information

Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

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