

DDR3 Sample Point Analyzer Quick Start

About this Quick Start Guide

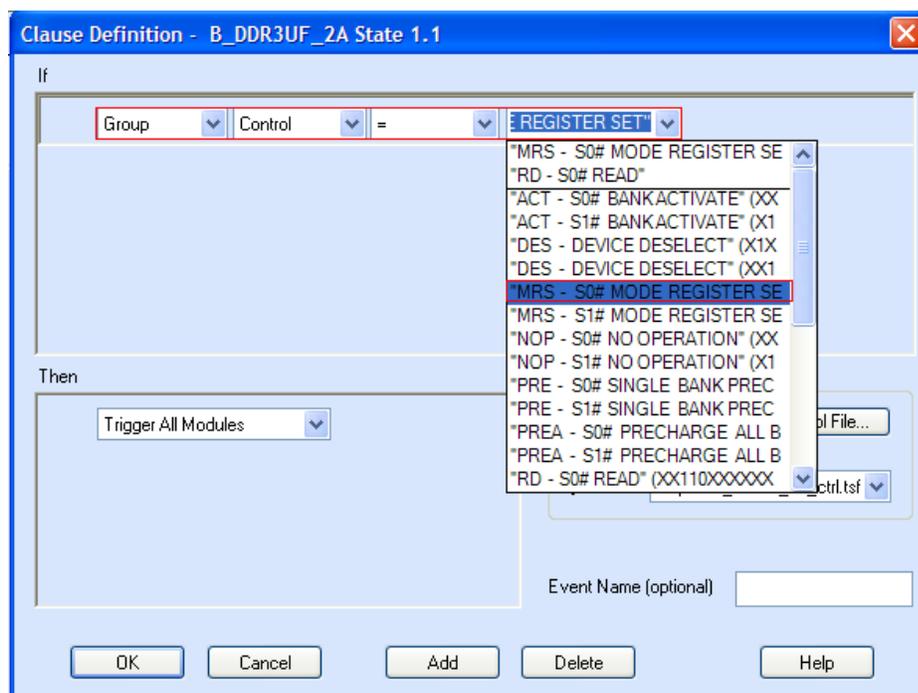
This guide will walk through the basic steps for using Nexus Technology DDR3 Sample Point Analyzer (SPA) to configure a Tektronix Logic Analyzer (TLA) for acquiring valid DDR3 data from a target.

NOTE: To properly function, the DDR3 SPA requires Tektronix TLA7BB4 modules, TLA software V5.4.044 or later. For best operation, TLA software version V5.5.108 or later is highly recommended.

NOTE: Before utilizing the DDR3 SPA, a Nexus Technology DDR3 Support must be loaded on the module selected.

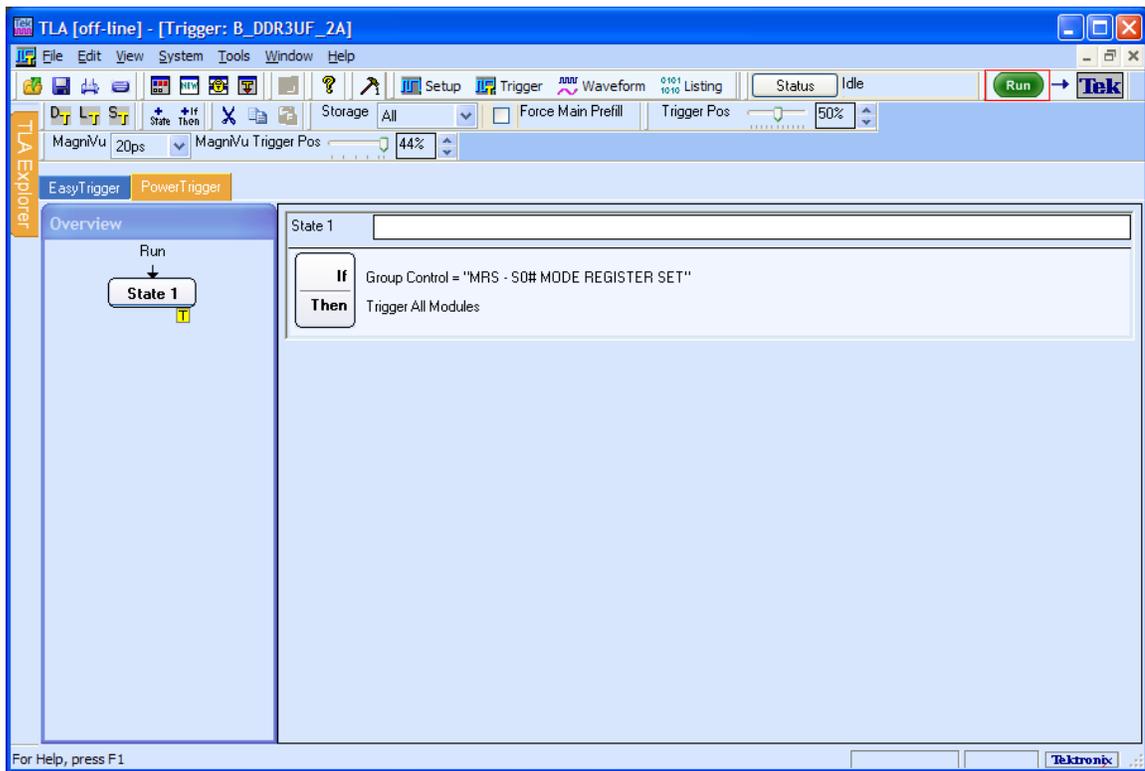
1. Trigger on a Mode Register Set from target.

Set the TLA to trigger on an MRS cycle:



2. Run the TLA.

Click the *Run* button.



3. Determine the configuration parameter values.

Locate the following parameter values (needed for Step 7):

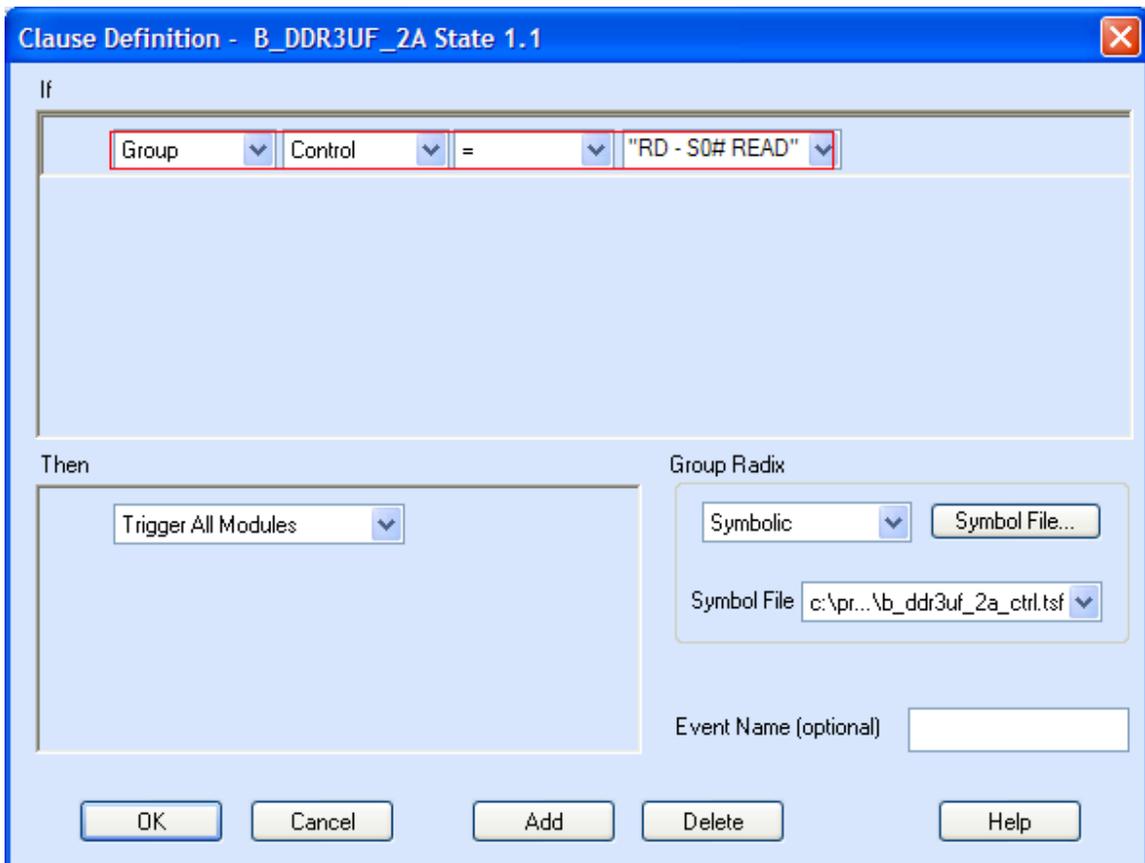
- CAS Latency
- CAS Write Latency
- CAS Additive Latency
- Burst Length
- Registered or Unregistered

The screenshot shows the TLA Explorer interface with a table of memory configuration parameters. The table has three columns: Sample, B_DDR3UE_2B Address, and B_DDR3UE_2B Mnemonics. The parameters are grouped into three samples, each with five rows of data. Red boxes highlight specific values: 'CAS Write Latency: 7' in the first sample, 'Additive Latency: 0' in the second sample, 'CAS Latency: 9' in the third sample, and 'Burst: 8 (fixed)' in the third sample.

Sample	B_DDR3UE_2B Address	B_DDR3UE_2B Mnemonics	
0	20010	(E)MRS - (EXTENDED) MODE REGISTER 2 (S0#)	
	20010	Rtt_WR: Dynamic ODT off	
	20010	Self-Refresh Range: Normal	
	20010	Auto_Self-Refresh Method: External	
	20010	CAS Write Latency: 7	
1	30000	(E)MRS - (EXTENDED) MODE REGISTER 3 (S0#)	
	30000	MPR: Normal Operation	
	30000	MPR Location: Predefined Pattern	
	2	10042	(E)MRS - (EXTENDED) MODE REGISTER 1 (S0#)
		10042	Output Buffer: Enabled
10042		TDQS: Disabled	
10042		Rtt_Nom: RZQ/2 (eff 120ohm)	
10042		Write Levelization: Disabled	
3	01D58	(E)MRS - (EXTENDED) MODE REGISTER 0 (S0#)	
	01D58	PD Mode: Fast Exit (DLL on)	
	01D58	Write Recovery: 12	
	01D58	DLL Reset: Yes	
	01D58	Operating Mode: Normal	
		Latency: 9	
		Burst Type: Interleaved	
		Burst: 8 (fixed)	

Trigger on Read or Write data from target.

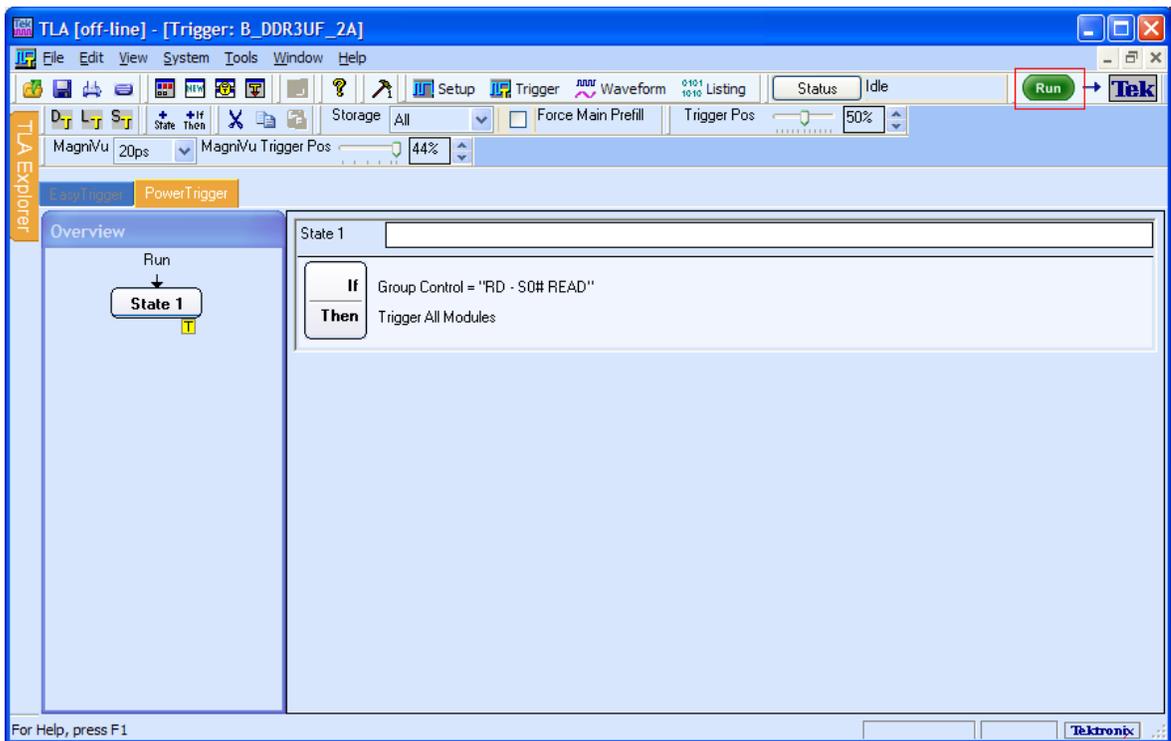
Set the TLA to trigger on a Read or a Write burst:



Data Requirements: To properly locate data eyes, the DDR3 SPA requires that alternating Read and Write commands are issued against all active Chip Selects.

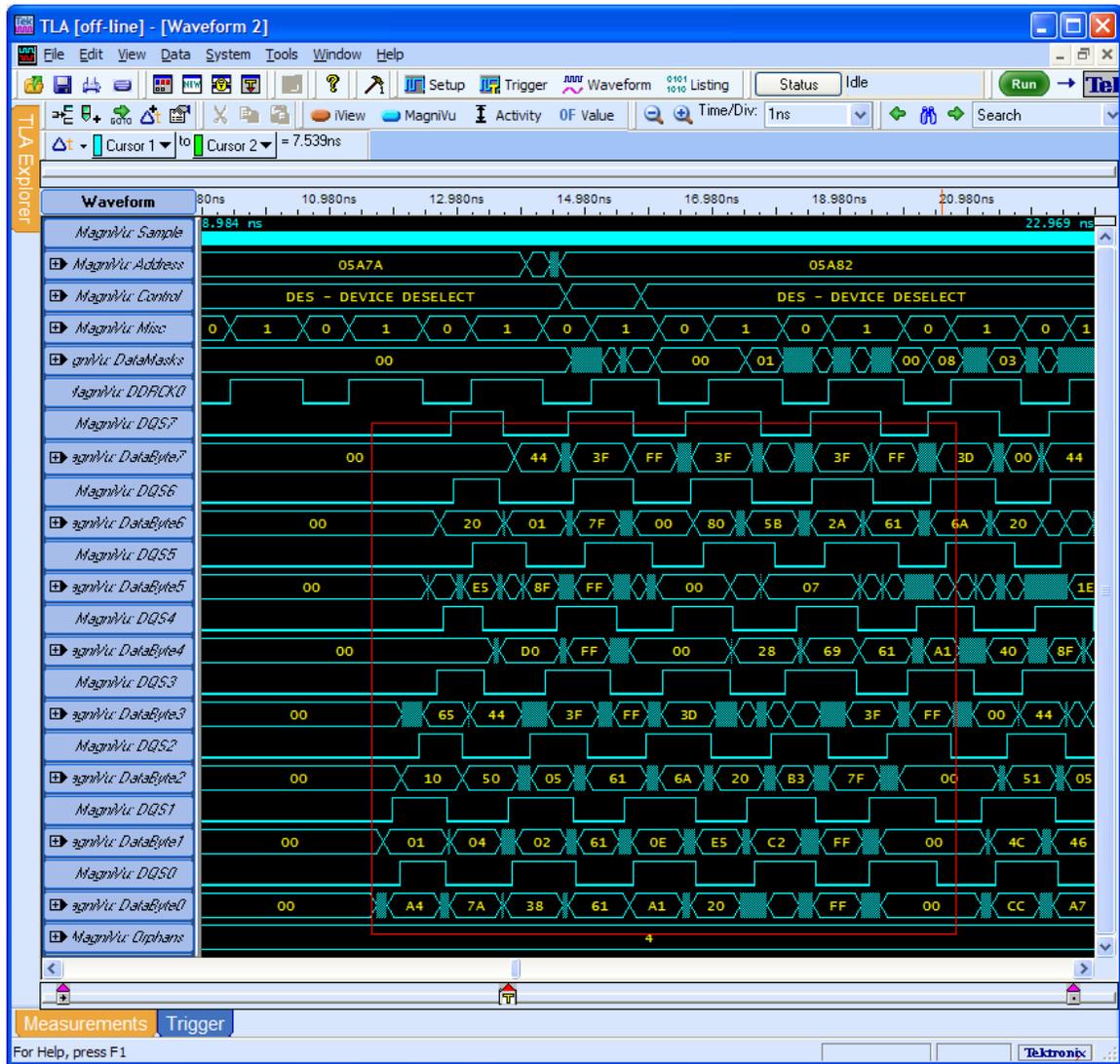
4. Run the TLA.

Click the *Run* button.



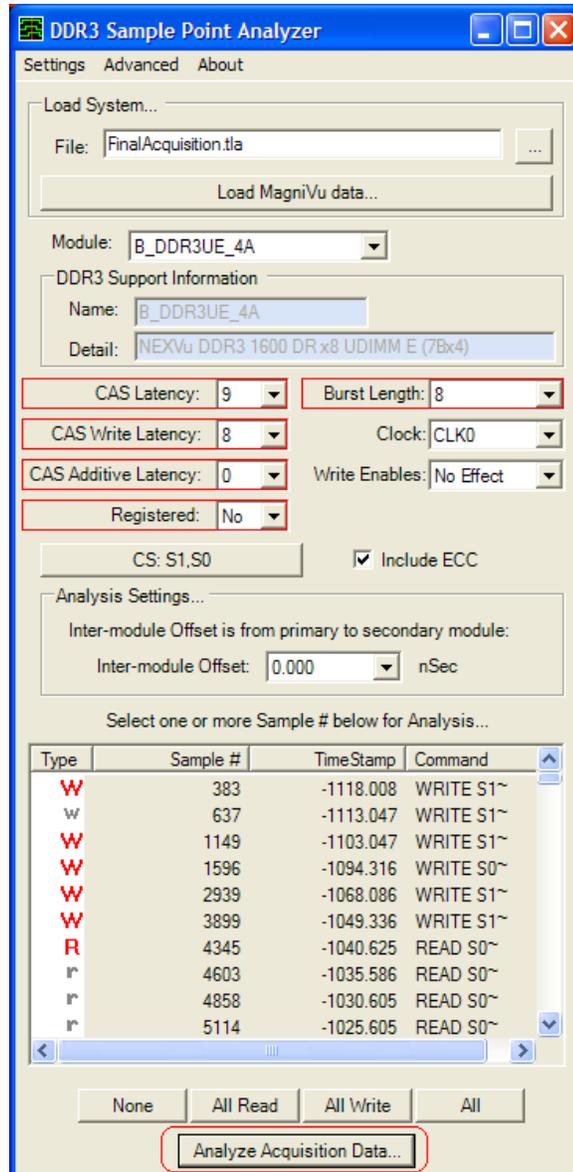
5. Review data acquired.

Ensure data transitions exist within the burst for all groups.



6. Run SPA and enter configuration parameters.

Double click the icon to start.



Set:

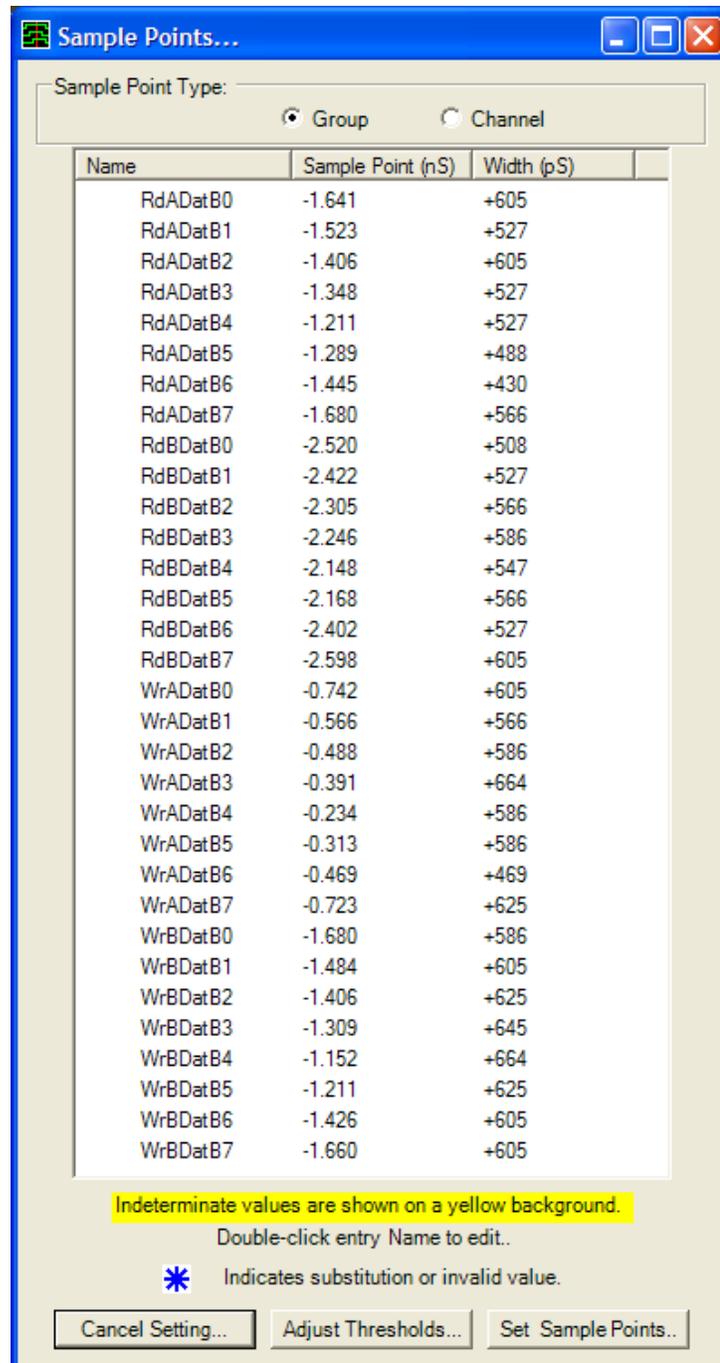
- CAS Latency
- CAS Write Latency
- CAS Additive Latency
- Burst Length
- Registered

The default values supplied for Inter-Module Offset and Active Chip Selects are acceptable for most configurations.

Click the *Analyze Data...* button.

7. Verify the data.

Verify valid values are displayed for all groups and click the *Set Sample Points...* button.



Congratulations, you are now ready to acquire valid DDR3 data from your target!

If the Sample Points that were displayed in the results dialog were invalid, additional tuning to your target may be necessary. Refer to the DDR3 SPA Tuning Guide and the DDR3 Sample Point Analyzer User's Manual Appendices C and D for details on additional tuning features.

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