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DDR4 PROTOCOL CHECKS

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DDR4 PROTOCOL CHECKS

Contents

Foreword

The intended use of this document is for the validation and debug of DDR4 based designs. This document contains protocol checks, sometimes referred to as memory access rules or protocol violations. These protocol checks can be implemented in simulation for pre-silicon verification or implemented in a protocol analyzer, logic analyzer, or oscilloscope for post silicon verification. The contained list of protocol checks is by no means the definitive list of protocol checks as other checks not contained in this list probably do exist.

This document was created by the JC-40.5 JEDEC Committee. This document is subservient to the JEDEC JESD79-4B DDR4 Specification and the SPD Specification, JESD 21-C Section Title: Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules.

DDR4 PROTOCOL CHECKS

(From JEDEC Board Ballot JCB-17-17, formulated under the cognizance of the JC-40.5 Subcommittee on Logic Validation and Verification.)

1 Scope

This document contains a list of checks that can be used during the verification or debug stages of development to check that accesses to a DDR4 DRAM adhere to JESD79-4B. These checks are derived from JESD79-4B. The intent of this document is not to supplant the JESD79-4B document, but to help consolidate the checks into a single easy to read document. This document was not intended to indicate *how* a protocol check measurement would be made, but *what* measurement would be made. The how can differ based on the testing requirements or the equipment at hand. This document is not a definitive list as other DDR4 protocol checks do exist and can be added to this document during subsequent revisions.

2 Normative reference

JESD79-4B, *DDR4 SDRAM Standard.*

3 Terms and definitions

For the purposes of this document, the following terms and definitions are used in this document.

Symbol: A shorthand notation per JESD79-4B for the Parameter.

NOTE Where the cell is grayed out, there is no official JEDEC parameter currently defined. However the equation is defined.

Parameter: A text description from JESD79-4B describing the time between events targeting the DDR4 DRAM.

Violation Criteria: in formula format is derived from the JESD79-4B specification. This is the protocol check. It is written such that if the condition is satisfied the protocol check fails and a violation exists.

Reference: A guide to the reader of where to look in JESD79-4B for more information on this protocol check. By no means is the reference exhaustive as the Parameter may be listed in many places. This is meant to be a starting point for the reader.

Units: How the protocol check will be measured.

Notes: Guidance as to special cases that concern that particular check and can be found in JESD79-4B.

4 DDR4 Protocol Checks – based on Timing between events

In general, the DDR4 specification details commands and the allowable time between those commands targeted to the DDR4 DRAM. Generally speaking, those commands cannot be too close or too far apart in time. A protocol check is the measurement to ensure that this is adhered to.

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
Read to Read Same Bank Group Write to Write Same Bank Group MPR page x to MPR page x (where x = 1,2 or 3)	tCCD_L	Measurement is less than tCCD_Lmin. tCCD_Lmin = MAX(tCCD_L{nCK}, ROUNDUP((tCCD_L{ns}/tCK{ns}) -.025))	Table 14, Table 132, Table 133, Figure 60, Figure 61, Section 4.10.3, 4.25.7	nCK	1,4
Read to Read Different Bank Group Write to Write Different Bank Group MPR page 0 to MPR page 0	tCCD_S	Measurement is less than tCCD_Smin.	Table 132, Table 133, Figure 60, Figure 61, Figure 82, Figure 83, Figure 117, Figure 118, Section 4.10.3, 4.25.7	nCK	1
Read to Write Same Bank Group Read to Write Different Bank Group		Measurement is less than CL - CWL + RBL/2 +1tCK + tWPRE	Section 4.25.6, Figure 84	nCK	1,3
Write to Read Same Bank Group		Measurement is less than CWL + WBL/2 + MAX(tWTR_L{nCK}, ROUNDUP((tWTR_L{ns}/tCK{nS}) -.025))	Section 4.25.6, Table 132, Table 133, Figure 65	nCK	1,3,4
Write to Read Different Bank Group		Measurement is less than CWL + WBL/2 + MAX(tWTR_S{nCK}, ROUNDUP((tWTR_S{nS}/tCK{nS}) -.025))	Section 4.25.6, Table 132 and Table 133, Figure 64	nCK	1,3,4
Activate to Activate Same Bank Group	tRRD_L	Measurement is less than tRRD_Lmin. tRRD_Lmin = MAX(tRRD_L{nCK}, ROUNDUP((tRRD_L{ns}/tCK{nS}) -.025))	Table 132, Table 133, Figure 62	nCK	1,2,4
Activate to Activate Different Bank Group	tRRD_S	Measurement is less than tRRD_Smin. tRRD_Smin = MAX(tRRD_S{nCK}, ROUNDUP((tRRD_S{ns}/tCK{ns}) -.025))	Table 132,133, Figure 62	nCK	1,2,4
Greater than 4 Activate commands window	tFAW	Measurement is less than tFAWmin. tFAWmin = MAX(tFAW{nCK}, ROUNDUP((tFAW{ns}/tCK{ns})-.025))	Table 132, Table 133, Figure 63	nCK	1,2,4

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
READ to PRE or PREA to the same Bank		Measurement is less than MAX((tRTP{nCK}, ROUNDUP(tRTP{ns}/tCK{ns}))+ AL	Section 4.24.3, Figure 98,Figure 100 Table 132, Table 133	nCK	1,3,7
WR to PRE or PREA to the same Bank If both DM and CRC are enabled		Measurement is less than WL + BL/2 + ROUNDUP((tWR{nS}/tCK{ns}) -.025) WL + BL/2 + MAX((tWR_CRC_DM{nCK}, ROUNDUP(tWR_CRC_DM{nS}/tCK{ns}))	Figure 131, Section 4.25.5, Table 132, Table 133	nCK	1,3,7
DLL locking time: DLL Reset (MR0 b8) to any command requiring a locked DLL or CKE low. Commands requiring a locked DLL; RD, RDS4, RDS8, RDA, RDAS4, RDAS8	tDLLK	Measurement is less than tDLLKmin.	Table 14, Table 132, Table 133, Section 3.3.1, Section 4.27, Figure 6	nCK	1
Mode Register Set command cycle time: MRS to MRS **Exceptions:** Gear Down Mode, C/A Parity Latency Mode, Per DRAM Addressability Mode, VrefDQ training value, mode and range, CS to Command/Address Latency Mode	tMRD	Measurement is less than tMRDmin.	Table 132, 133. Figure 8, Section 3.4.1	nCK	1
Mode Register Command update delay: MRS to non-MRS Command or ODT high **Exceptions are listed in Note 2 Figure 9.**	tMOD	Measurement is less than tMODmin. tMOD = MAX(tMOD{nCK}, ROUNDUP(tMOD{ns}/tCK{ns}))	Table 132,133, Section 3.4.1, Figure 9, Figure 11 ODT reference 4.7.2 and Figure 15	nCK	1,7
Powerup and Reset calibration time: 1st ZQCL after Reset Low to High to any Command, ODT high, or CKE Low	tZQinit	Measurement is less than tZQinitmin.	Table 132, Table 133, Figure 6, Figure 26	nCK	1
Normal Operation full calibration time: All but the 1st ZQCL after Reset Low to High to any Command, ODT high, CKE Low	tZQoper	Measurement is less than tZQopermin.	Table 132, Table 133, Figure 26	nCK	1
Normal Operation short calibration time: Time from ZQCS to any Command, ODT high, CKE Low	tZQCS	Measurement is less than tZQCSmin.	Table 132, Table 133, Section 4.12.1, Figure 26	nCK	1

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
RESET_n Low to High, then CKE Low to High to a valid Command	tXPR	Measurement is less than tXPRmin. tXPRmin = MAX(tXPR{nCK}, ROUNDUP((tRFCmin+10{ns})/tCK{ns})-.025))	Table 24, Table 132, Table 133, Figure 6, 7, Section 3.3.1	nCK	1,4
SRX to Commands not requiring a locked DLL Commands not requiring a locked DLL: ACT, PRE, PREA, REF, SRE, PDE,WRITE On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period.	tXS	Measurement is less than tXSmin. tXSmin = ROUNDUP((tRFCmin+10ns)/tCK{ns})-.025)	Table 24, Table 132 and Table 133, Figure 11, Figure 12, Section 4.4.3 Section 4.4.2, 4.27 Note 8: Section 4.2	nCK	1,4
SRX to any command not requiring a locked DLL in self refresh ABORT Commands not requiring a locked DLL: ACT, PRE, PREA, REF, SRE, PDE, WRITE Disable this check if MR4 A9 is not set (Disable Self Refresh Abort)	tXS_ ABORT	Measurement is less than tXS_ABORTmin. tXS_ABORTmin = ROUNDUP(((tRFC4+10ns)/tCK{ns})-.025)	Table 24, Table 132 and Table 133, Figure 11, Figure 12, Section 4.4.3 Section 4.4.2, 4.27 Section 3.5	nCK	1,4
SRX to ZQCL, ZQCS and MRS	tXS_ FAST	Measurement is less than tXS_FAST. tXS_FASTmin = ROUNDUP((tRFC4+10ns)/tCK{ns})	Table 132 and Table 133, Section 4.4.2	nCK	1,7
SRX to Commands requiring a locked DLL, READ or CKE Low or ODT High (synchronous ODT Commands)	tXSDLL	Measurement is less than tXSDLLmin tXSDLL = tDLLK(min)	Table 132 and Table 133, Section 4.27 #2, Figure 146, Note 8 Section 4.2	nCK	1
Exit Power Down with DLL on to any valid Command Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL Exit Power Down to ODT =1: MR5 A5=0 (ODT enabled)	tXP	Measurement is less than tXPmin. tXPmin = MAX(tXP{nCK}, ROUNDUP(tXP{ns})/tCK{ns})	Table 132 and Table 133. Figure 45, Figure 46, Figure 148, Table 56 Table 132 and Table 133 Figure 184	nCK	1,7

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
Even Parity is present on PAR, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0, and C0-C2 for 3DS. Only when MR5 A2:0 is NOT 000 Only when DLL mode is enabled		ODD number of 1's present when Parity Enabled.	Section 2.7, Table 13, Section 3.5 Section 4.5	integer number	3
Minimum CKE low width for Self refresh entry to exit timing This is the minimum amount of time the DRAM must stay in Self Refresh	tCKESR	Measurement is less than tCKESRmin. tCKESRmin = tCKEmin + 1nCK	Table 132 and Table 133, Figure 146 Section 4.27	nCK	1
CKE minimum pulse width (low and high)	tCKE	Measurement is less than tCKEmin. tCKEmin = MAX(tCKE{nCK}, ROUNDUP(tCKE{ns})/tCK{ns}))	Table 132 and Table 133 and Note 31 and Note 32. Figure 158	nCK	1,7
Power Down entry to exit timing minimum	tPDmin	Measurement is less than tPDmin. tPDmin = MAX(tCKE{nCK}, ROUNDUP(tCKE{ns})/tCK{ns}))	Table 132 and Table 133. Figure 45, Figure 158	nCK	1,7
Power Down entry to exit timing maximum ODT must be stable prior to Power Down entry and remain stable throughout	tPDmax	Measurement is greater than tPDmax. tPDmax=Roundup (9*tREFI{ns})/tCK{ns})	Table 132 and Table 133. Figure 45, Figure 158 Figure 148, Figure 149	nCK	1,7
Timing of ACT command to Power Down entry	tACTPDEN	Measurement is less than tACTPDENmin.	Table 132 and 133, Figure 155	nCK	1
Timing of PRE or PREA command to Power Down entry	tPRPDEN	Measurement is less than tPRPDENmin.	Table 132 and 133. Figure 156	nCK	1
Timing of RD or RDA command to Power Down entry	tRDPDEN	Measurement is less than tRDPDENmin. tRDPDENmin = RL + 4 + 1	Table 132 and 133. Figure 150	nCK	1
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	Measurement is less than tWRPDENmin. tWRPDENmin = WL + 4 + ROUNDUP((tWR{ns}/tCK{ns})-.025)	Table 132 and 133. Figure 152	nCK	1,4

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF). WR in clock cycles as programmed in MR0	tWRAPDEN	Measurement is less than tWRAPDENmin. tWRAPDENmin = WL + 4 + WR + 1	Figure 151, Table 132 and Table 133 Note 5	nCK	1
Timing of REF command to Power Down entry	tREFPDEN	Measurement is less than tREFPDENmin. tREFPDENmin = tREFPDENmin	Table 132 and Table 133. Figure 154	nCK	1
Timing of MRS command to Power Down entry	tMRSPDEN	Measurement is less than tMRSPDENmin. tMRSPDENmin = tMOD(min)	Table 132 and Table 133. Figure 157	nCK	1
Activate to PRE command period Minimum	tRASmin	Measurement is less than tRASmin tRASmin = ROUNDUP((tRASmin{ns}/tCK{ns})-.025)	Tables 107-113	nCK	1,4
Activate to PRE command period Maximum	tRASmax	Measurement is greater than tRASmax tRASmax = ROUNDUP(9*tREFI{ns}/tnCK{ns})	Tables 107 - 113	nCK	1,7
ACT to Read or Write Delay Time	tRCD	Measurement is less than tRCD tRCD = ROUNDUP((tRCD{ns}/tCK{ns})-.025)	Tables 107 - 113	nCK	1,4
ACT to ACT or REF command period	tRC	Measurement is less than tRC tRC = ROUNDUP((tRC{ns}/tCK{ns})-.025)	Tables 107 - 113	nCK	1,4
REF to a non-Deselect Command	tRFC1, tRFC2, tRFC4	Measurement is less than tRFCxmin tRFCx = ROUNDUP((tRFCx{ns}/tCK{ns})-.025)	Section 4.26, 4.9.2, Table 24, 132, 133. Figure 143	nCK	1,5,4
Average Refresh Interval	tREFI1, tREFI2, tREFI4	Measurement equal or less than tREFIx measured over 8192 intervals with a rolling window.	Section 4.8.1, 4.8.2, 4.9.1,4.9.2, 4.26. Table 24,131	nCK	1,6,7
Maximum time between Refreshes	tREFI max	Measurement equal or less than 9*tREFI.	Table 24,131 Section 4.26, Figure 143	nCK	5,6,7
Timing of a WR command to Power Down Entry (BC4MRS)	tWRPBC4DEN	Measurement is less than tWRPBC4DEN. tWRPBC4DEN = WL + 2 + ROUNDUP((tWR/tCK) -.025)	Table 132,133	nCK	1,4
Timing of a WRA command to Power Down Entry (BC4MRS)	tWRAPBC4DEN	Measurement is less than tWRAPBC4DEN. tWRAPBC4DEN = WL + 2+ WR + 1	Table 132,133	nCK	1

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
PRE or PREA to ACT, ZQCS, ZQCL, MRS, REF, SRE	tRP	Measurement is less than tRP tRP = ROUNDUP((tRP{ns}/tCK{ns})-.025)	4.12.1, 4.23, 4.26, 4.27, Figure 18, 21, 23, 98-102. Table 107-113	nCK	1,4
RDA to ACT same Bank, ZQCS,ZQCL,MRS,REF, SRE same Rank Command Timing		Measurement is less than AL+ ROUNDUP(tRTP{ns}/tCK{ns}) + ROUNDUP((tRP{ns}/tCK{ns})-.025)	Figure 102, Table 132, 133	nCK	1,3,4,7
WRA to ACT in Same Bank WRA to ZQCS, ZQCL, MRS, REF, SRE in Same Rank		Measurement is less than WL+ BL/2+ WR+ROUNDUP((tRP/tCK)-0.025)	Section 3.5. Table 132,133. Figure 134,133	nCK	1,3,4
Command Pass disable delay (delay time after SRE and PDE for DRAM to block input signals) ODT during tCPDED	tCPDED	Measurement is not equal to all DES commands during tCPDED. ODT not stable during tCPDED	Table 132-133. Section 4.28.1. Figure 45, 50, 148, 146, 183	nCK	1
Minimum ODT assertion time BC4 (Fixed)	ODTH4	ODT minimum assertion time is less than ODTH4.	Section 5.2.2, Table 75, Figure 177	nCK	
Minimum ODT assertion time BC8, BC4 (OTF)	ODTH8	ODT minimum assertion time is less than ODTH8.	Section 5.2.2, Table 75, Figure 177	nCK	

NOTE 1 For the appropriate Speed Bin.
NOTE 2 Based on Page Size: 2K, 1K, 1/2K.
NOTE 3 Gray colored indicates symbol not found in JEDEC document.
NOTE 4 The 2.5 % Rounding Algorithm was passed in March of 2016 and applies only to those parameters stored in the SPD.
NOTE 5 Varies with Density.
NOTE 6 Dependent on Operating Temperature.
NOTE 7 This Roundup is a simple roundup without a guardband.

5 DDR4 Protocol Checks – Based on Ordering of Events

In general, the DDR4 specification details commands and their allowable order relative to other commands. A protocol check is the measurement to ensure that this is adhered to.
This Protocol Checks chart gives the following information:

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
Read or Write to an Inactive Bank		Read or Write to a closed or inactive Bank	Section 3.1, 3.2, 4.22		1
Refresh to an Active Bank		All Banks must be Precharged or closed prior to REFRESH	Section 3.1, 4.26		1
Activate to an Active bank		ACTIVATE Command to an Active Bank	Section 3.1, 4.22		1
MRS with an Active Bank		MRS Command with an ACTIVE Bank	Section 3.1		1
Self Refresh Entry with an Active Bank		Self Refresh Entry with an ACTIVE Bank	Section 4.2, 3.1		1
ZQCS or ZQCL with an Active bank		ZQCS or ZQCL Command with an ACTIVE Bank	Section 3.1, 4.12.1		1

NOTE 1 These are Ordering Checks.

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1. I recommend changes to the following:

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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☐ Other _____

2. Recommendations for correction:

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3. Other suggestions for document improvement:

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