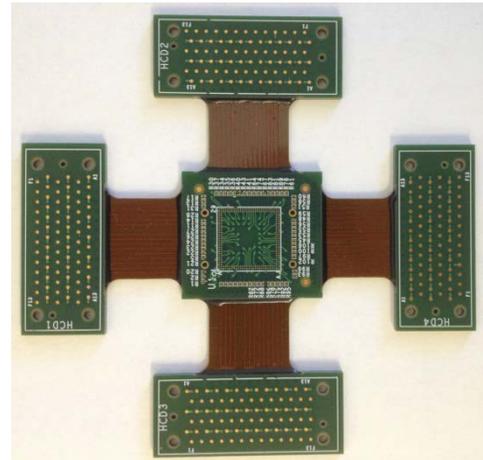


LPDDR3 PoP Logic Analyzer Component Interposer

216 ball Package on Package memory device support

- Optimal Digital Validation
- Easy to Install
- Use with existing Embedded / Mobile designs
- Socket Design – also available without a socket
- Support for LPDDR3 Memory Devices
 - Package on Package (PoP)
 - 12mm X 12mm
 - 2x32 data width
 - 0.4 mm pitch
- Probed at the BGA Pads
- TLA setup software (iCiS) included
- Optional Compliance Analysis software available
- Compatible with Nexus Memory Compliance Analyzer (MCA) Instrument



Nexus Technology recommends LPDDR3 component interposers for applications requiring optimal digital validation of LPDDR3 targets. These interposers allow for logic analyzer acquisition of command, address, and data of 216-ball LPDDR3 components. These interposers are also compatible with the Nexus MCA Instrument.

The PoP Challenge

Low Power DDR3 memory components are expanding rapidly in the market providing low power, high bandwidth, high density memory solutions. The Package on Package version results in target space saving but introduces significant roadblocks for test/debug and analysis of the memory interface.



Figure 1 - Side view (photo) of PoP memory soldered on to a processor

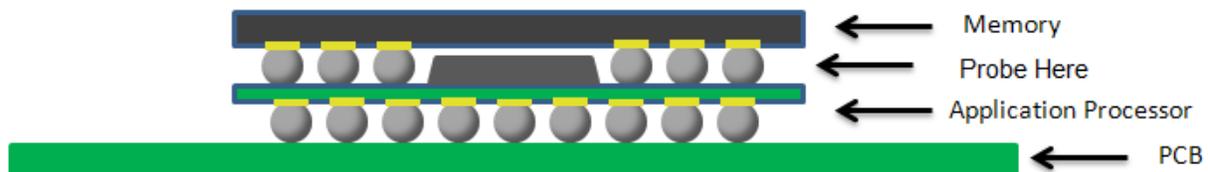


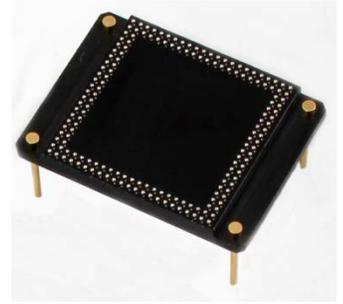
Figure 2 - Side view (drawing) of the PoP memory soldered onto a processor

Premier Component Interposer Design

Optimal LPDDR3 validation requires analysis of the LPDDR3 signals, as seen by the memory components. This allows for the highest confidence that the captured signals are representative of the signals on the target. Nexus Technology component interposers allow for logic analyzer probing of the LPDDR3 signals at the memory components BGA balls.

Memory Component Interposer Installation

The process of attaching the interposer to your target has been greatly simplified using Nexus Technology's patented, high-bandwidth, component interposer sockets. These patented sockets remove the need to contract specialized rework houses to perform the installation. Instead, you can use standard BGA assembly practices to install the component interposer socket. Nexus Technology can perform the attachment service for a nominal fee.



Once the interposer socket is installed on the target, logic analyzer or oscilloscope, interposers can be easily inserted or removed from the socket. Note that the interposer socket elevates the interposer above the adjacent components to provide the mechanical clearance necessary for easy probe attachment.

LPDDR3 BGA Component installation

The interposer can be ordered with a socket on the interposer for easy BGA memory component installation and removal. These sockets allow for the quick swapping and testing of different memory components on the interposer. [The Sockets quick Start Guide](#) provides more information.

LPDDR3 PoP Logic Analyzer Component Interposer

Logic Analyzer Component Interposer Hardware

Connection to a logic analyzer is enabled by using LPDDR3 Memory Component Interposers. These controlled impedance, matched trace length interposers provide visibility for digital validation using a logic analyzer. The rigid / flex / rigid design allows for the interposer to be used in targets with minimal mechanical clearance around the target component. These interposers are also compatible with the Nexus MCA Instrument.

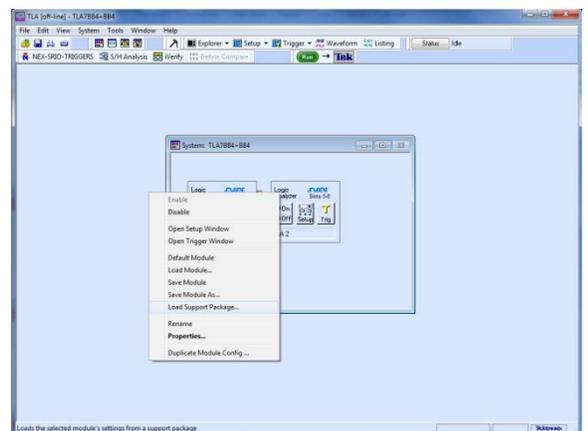
Logic Analyzer Component Interposer Software

Nexus Technology component interposers come with the required logic analyzer setup software and iCiS setup tool. Optional full compliance analysis software is available separately.

Logic Analyzer Setup Software

The Logic analyzer setup software provides a quick setup of the clocking / acquisition parameters. This software also includes protocol decoding of the LPDDR3 transactions for easy display and analysis. Setup is fast and easy using the graphical iCiS Tool.

- Load the TLA Software
- Load the Support Package
- Run the calibration tools
- Ready to Acquire!



TLA Data Analysis

Synchronous state data correlated with 50GHz MagniVu timing data, iCapture Analog Mux, and Compliance Analysis tools provide analysis capability that is best in the industry.

Bus Decode and Timing

The logic analyzer provides listing and timing displays of the synchronous state and asynchronous MagniVu timing data. The MagniVu timing data is acquired simultaneously and is correlated to the state acquisition data with no skew. In fact, the state acquisition data is derived from the MagniVu timing data. This provides much more information on the acquired data and, most importantly, it provides an extra level of confidence that the data acquired was correct.

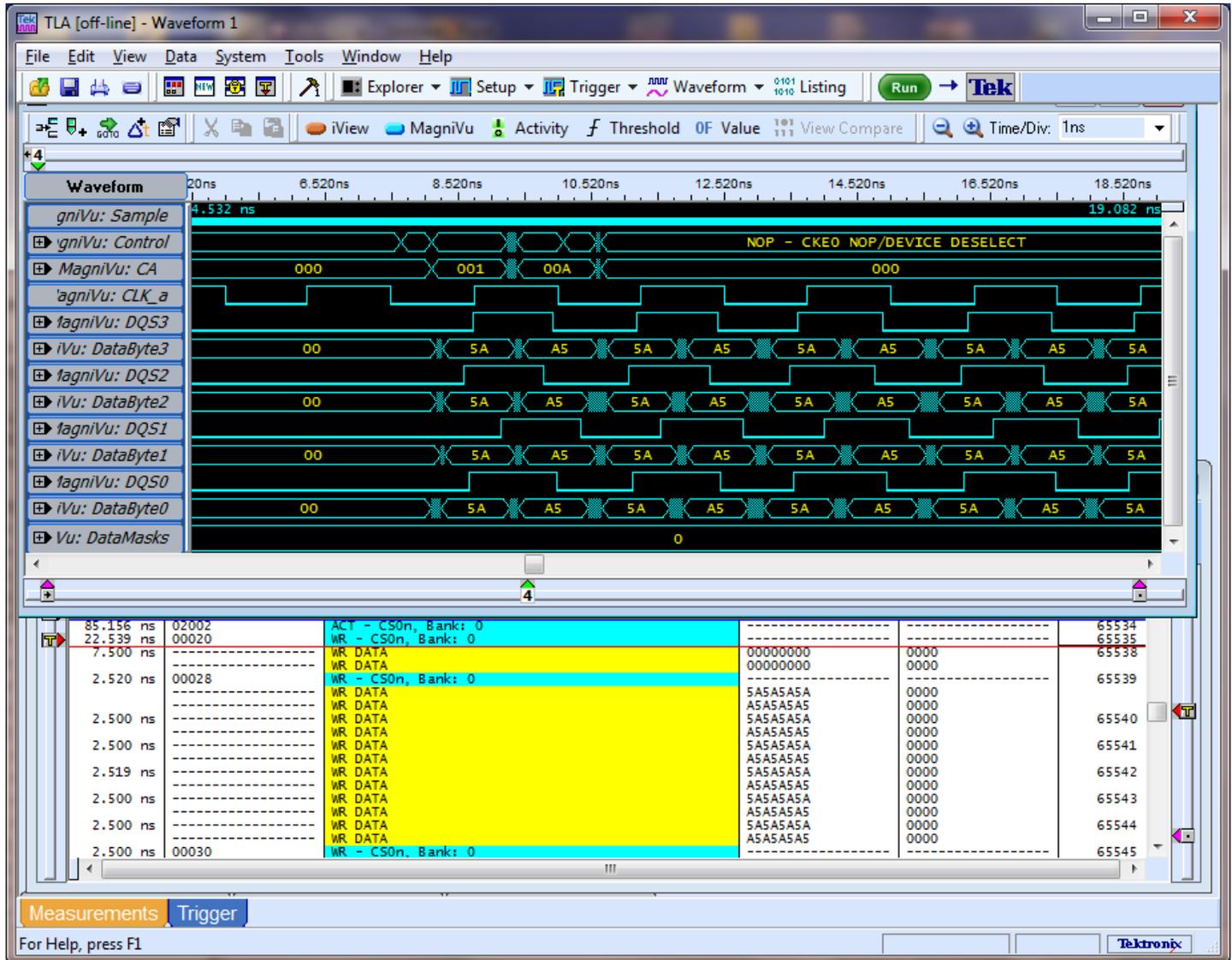


Figure 3 - State & 50GHz MagniVu Timing

The asynchronous, 50GHz (20ps) MagniVu timing data provides extremely accurate timing analysis of the LPDDR3 bus and is simultaneously acquired and correlated with the state acquisition data.

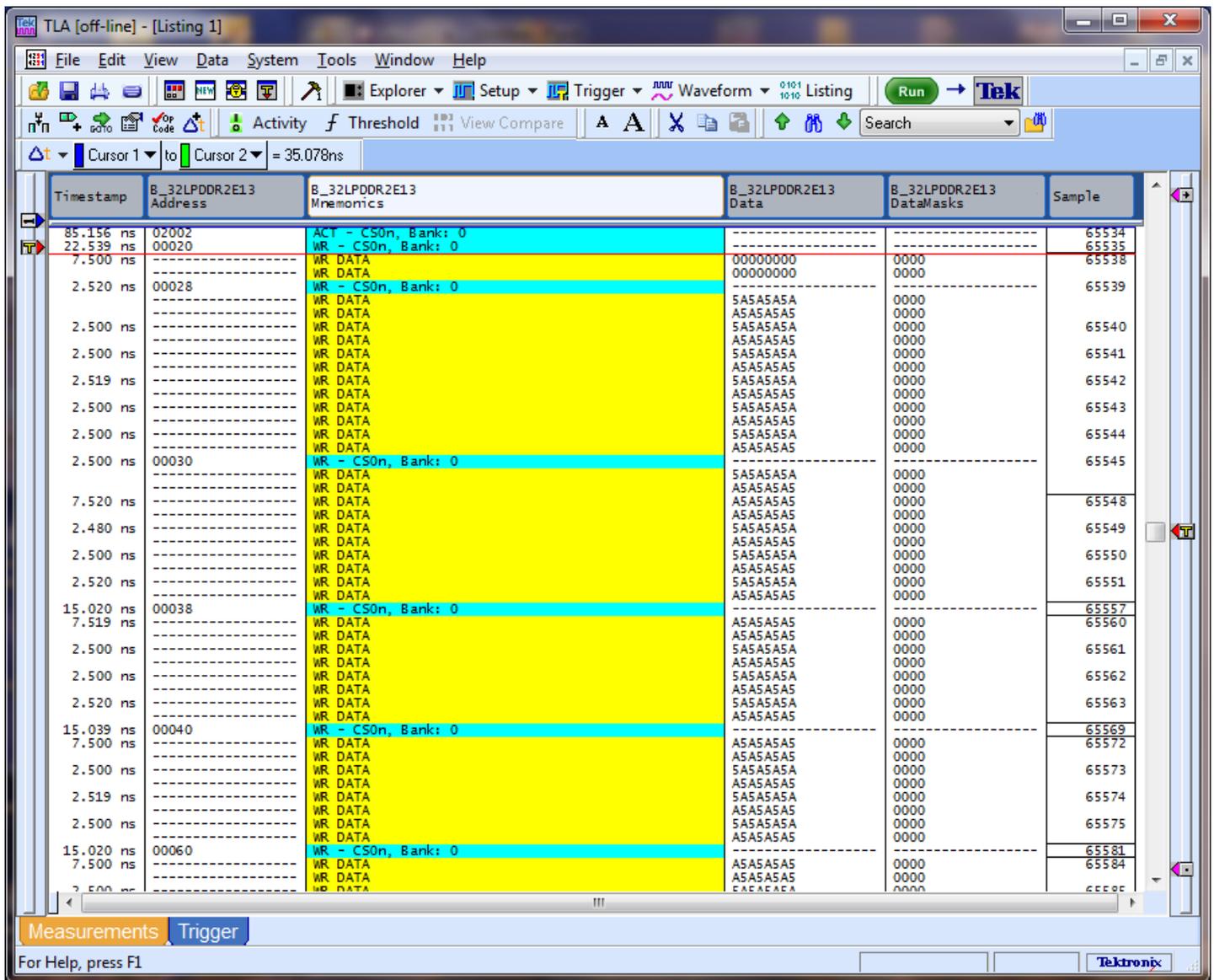


Figure 4 - State Data

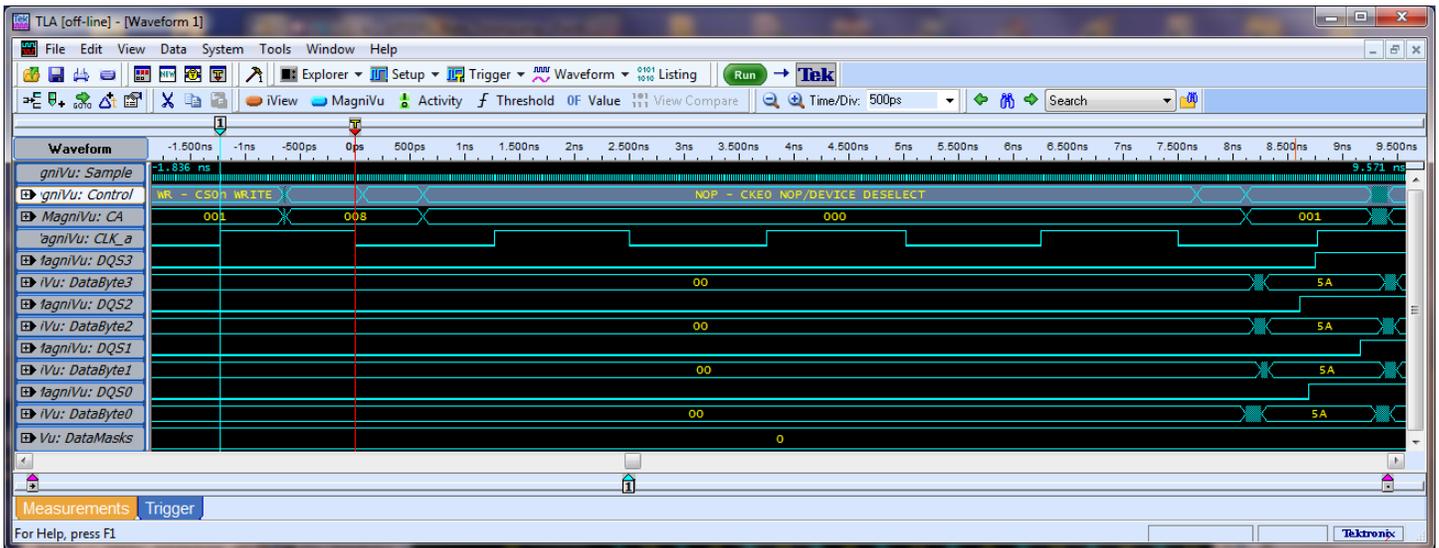


Figure 5 - MagniVu Timing Data

iCapture Analog Mux

A powerful analog validation feature is the Tektronix Logic Analyzer's unique Analog Mux capability. This provides the ability to see *any* channel of the LPDDR3 bus in seconds on an oscilloscope. This is invaluable information which allows analysis within minutes as to the status and behavior of the LPDDR3 bus. No extra probing is required! This information can be pushed back into the logic analyzer, correlated and viewed in a wave form window along with the state or timing data using the iView Feature.

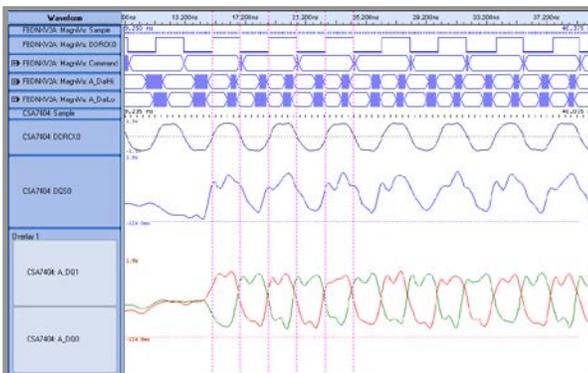


Figure 6 - Example Representation of iView

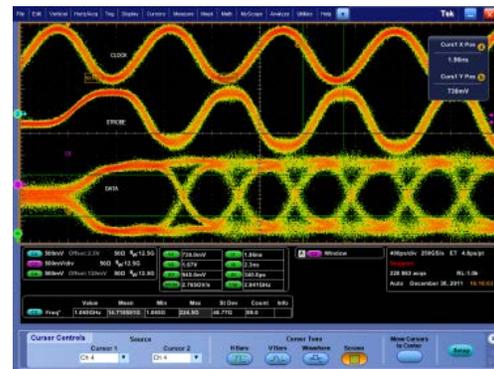


Figure 7 - Example iCapture Analog Mux

Taking advantage of the ultra-high fidelity "Scope Probe per Signal" capability of the LPDDR3 Interposer, iCapture enables focused analog level analysis and validation.

Sample Point Setup

In order for the logic analyzer to capture signals accurately, the sample points must be properly set. iCiS provides a graphical display of the signal eyes on a per group or per signal basis (See Figure 6). You easily select the optimum sample point.

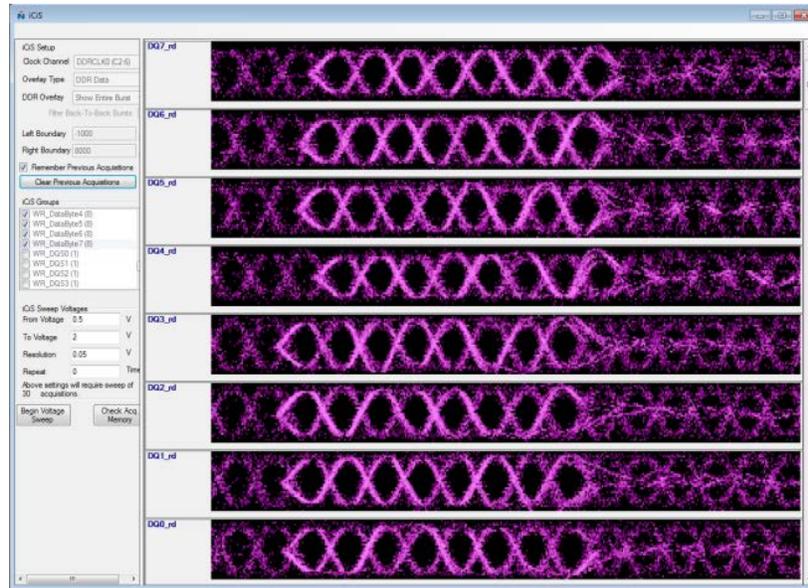


Figure 8 - Example iCiS DQ Data Setup

Setting up the logic analyzer is easy! Load the TLA software, load the support package, and click Run. It's as simple as that for compliance analysis (CMD/ADDR/CTRL acquisition). Acquiring the DQ read and write data is easily done with the graphical iCiS tool.

Compliance Analysis Software

These products optionally include the LPDDR3 Memory Compliance Analysis software package. This software performs advanced command sequence & timing compliance analysis. It also provides statistical information and global bus activity to quickly give the user an overview of the LPDDR3 bus activity without having to revert to a listing or waveform window.

- Extensive JEDEC LPDDR3 Compliance Analysis
- Quick and Easy Setup w/No Calibration Required
- Automated Acquisition and Measurement
- Powerful in-application graphical and tabular analysis results
- Memory controller & JEDEC parameters predefined
- Quickly navigate through multiple acquisitions



	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R1 R0	NA	NA	NA	NA	959,880
R2 R1 R0	28,007	10,273,985	2,106,353	6.7	26,250
R3 R1 R0	7,441	878,808	123,227	3.3	7,200
R2 R1 R0	NA	NA	NA	NA	5,625
R1 R0	NA	NA	NA	NA	70,200,000
R2 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
R3 R1 R0	114,121	8,169,101	6,001,631	3.7	110,000
R2 R1 R0	42,969	2,839,180	267,945	14.6	37,500
R3 R1 R0	42,969	2,839,180	267,945	-99.9	70,200,000
R2 R1 R0	18,652	116,172	20,254	42.1	13,125
R3 R1 R0	13,066	316,308	170,537	16.1	11,250
R1 R0	NA	NA	NA	NA	20,625
R2 R1 R0	37,383	326,054	162,946	10.8	33,750

Figure 9 - Tabular Results Detail of Compliance Analysis

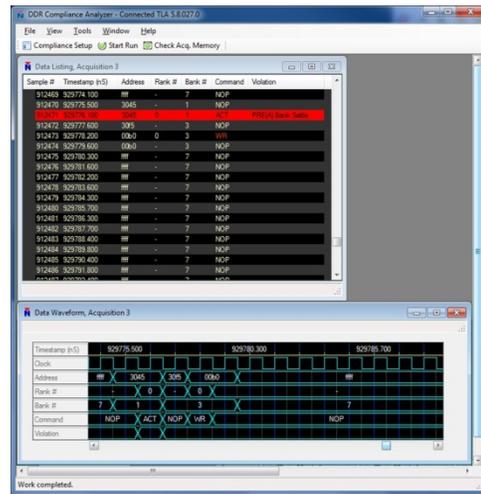


Figure 10 - Waveform & Timing Displays of Compliance Analysis

Stat	Num.	Name	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)	Description
1	0	CHD wh/SREF Bank	0	0	0	NA	NA	NA	NA	0	Sequential check. A non-NOP/DCS command can not occur on a self-refreshing bank.
2	0	SRE wh/ACT Bank	0	0	0	NA	NA	NA	NA	0	Sequential check. A Self Refresh Entry (SRE) command can not occur on an active bank.
3	0	MRS wh/ACT Bank	0	0	0	NA	NA	NA	NA	0	Sequential check. An Mode Register Set (MRS) command can not occur on an active bank.
4	0	RDAA/WRRA during MRS	0	0	0	NA	NA	NA	NA	0	Sequential check. A read (RD) or write (WR) command can not occur during rank MRS cycle.
5	0	CHD wh/REF Bank	0	0	0	NA	NA	NA	NA	0	Sequential check. A non-NOP/DCS command can not occur on a powered-down bank.
6	0	RDAA/WRRA wh/REF Bank	0	0	0	NA	NA	NA	NA	0	Sequential check. A read (RDAA) or write (WRRA) command can not occur during bank refresh.
7	32	ACT/REF wh/ACT Bank	32	32	0	0	0	0	0	0	Sequential check. A activate (ACT) or refresh (REF) command can not occur on an active bank.
8	0	REF wh/ACT Bank	0	0	0	NA	NA	NA	NA	0	Sequential check. A refresh (REF) command can not occur on an active bank in a reading or writing operation.
9	56	RDAA/WRRA to ePRE Bank	56	56	0	0	0	0	0	0	Sequential check. A read (RDAA) or write (WRRA) command can not occur during an inactive (charged) bank.
10	876	h/ACT	876	876	0	20,977	14,559,502	629,702	-29.3	27,000	Power-Down Exit (SPO/PPD) to any valid command (PRE/REF/ACT/MRS/SRE) must meet tPP.
11	0	PD Exit	0	0	0	NA	NA	NA	NA	6,000	Self Refresh Exit (SPO/PPD) to any command not requiring a locked DLL (PRE/REF/ACT/MRS/SRE) must meet tDS.
12	1,631	h/ACT	1,631	1,631	0	6,679	14,676,602	106,733	33.6	5,000	Minimum time from a PRE/ACT command to any valid command on the same bank (MRS/SRE) must meet tPP.
13	0	PRE/ACT Bank Settle	0	0	0	NA	NA	NA	NA	11,700	Sequential check. At least one refresh (REF) command is required between self refresh (SRX to SRE).
14	0	REF Before SRE	0	0	0	NA	NA	NA	NA	0	Sequential check. If the last valid command received before a self-refresh entry (SRE) was any precharge (PRE/A), then the separation between these two commands must meet tPRE.
15	0	SRE Separation from PRE(A)	0	0	0	NA	NA	NA	NA	1,018	If the last valid command received before a self-refresh entry (SRE) was a write (WR) or read (RD), then the separation between these two commands must meet tSRE.
16	0	SRE Separation from REF	0	0	0	NA	NA	NA	NA	1,018	If the last valid command received before a self-refresh entry (SRE) was a refresh (REF), then the separation between these two commands must meet tSRE.
17	0	SRE Separation from ACT	0	0	0	NA	NA	NA	NA	1,018	If the last valid command received before a self-refresh entry (SRE) was a activate (ACT), then the separation between these two commands must meet tSRE.
18	0	SRE Separation from MRS	0	0	0	NA	NA	NA	NA	15,000	If the last valid command received before a self-refresh entry (SRE) was a mode register set (MRS), then the separation between these two commands must meet tSRE.
19	0	SRE Separation from WR	0	0	0	NA	NA	NA	NA	22,486	If the last valid command received before a self-refresh entry (SRE) was a write (WR), then the separation between these two commands must meet tSRE.
20	0	SRE Separation from RD	0	0	0	NA	NA	NA	NA	25,450	If the last valid command received before a self-refresh entry (SRE) was a read (RD), then the separation between these two commands must meet tSRE.
21	0	SRE Separation from WR(A)	0	0	0	NA	NA	NA	NA	25,450	If the last valid command received before a self-refresh entry (SRE) was a write (WR(A)), then the separation between these two commands must meet tSRE.
22	0	SRE Separation from RD(A)	0	0	0	NA	NA	NA	NA	14,500	If the last valid command received before a self-refresh entry (SRE) was a read (RD(A)), then the separation between these two commands must meet tSRE.
23	0	MRS Settle	0	0	0	NA	NA	NA	NA	15,000	Minimum time from a mode register set (MRS) command to any other valid command that is not an MRS must meet tMRS.
24	0	MRS Burst	0	0	0	NA	NA	NA	NA	15,000	Minimum time from the first to the next and subsequent mode register set (MRS) commands must meet tMRS.
25	0	eSREF Time	0	0	0	NA	NA	NA	NA	6,000	The minimum amount of time in self-refresh must meet tCSESR.
26	1,536	WR to WR(A) Separation	1,536	1,536	0	4,936	2,592,000	27,200	-2.5	4,931	The minimum amount of time between write (WR) commands must meet tCDD.
27	0	RD to WR(A) Separation	0	0	0	10,156	127,949	11,225	42.5	7,105	The minimum amount of time between read (RD) and write (WR(A)) commands must meet tRWT.
28	0	PD Exit	0	0	0	NA	NA	NA	NA	24,000	Power-Down Exit (SPO/PPD) Slow Exit (MRS_AZ bit low) to read (RD(A)) command must meet tPDLL.
29	0	Bank DLL Reset to RD(A)	0	0	0	NA	NA	NA	NA	924,072	Power-Down Exit (SPO/PPD) to any valid command (PRE/REF/ACT/MRS/SRE) must meet tPPD.
30	43	WR to RD(A) Separation	43	43	0	18,896	14,593,211	149,106	-2.4	19,342	The minimum amount of time between write (WR) and read (RD(A)) commands must meet tRWT.
31	2,360	RD Burst	2,360	2,360	0	4,022	14,594,216	149,106	-1.2	4,041	The minimum amount of time between read (RD(A)) commands must meet tCDD.
32	0	eSREF Time	0	0	0	NA	NA	NA	NA	3,600	The minimum amount of time between read (RD(A)) commands must meet tCDD.
33	0	RD Time Max.	0	0	0	NA	NA	NA	NA	70,200,000	The maximum amount of time a bank can stay active (ACT to PRE(A)) must meet tPACT.
34	17,960	PRE(A) Bank Settle	17,960	17,960	0	19,111	366,351	26,166	-29.1	30,000	Minimum time from a PRE(A) command to any valid command on the same bank must meet tPACT.
35	0	h/REF Time	0	0	0	NA	NA	NA	NA	30,000	Minimum time from a REF command to any valid command on the same bank must meet tPREF.
36	0	h/ACT Time Min.	0	0	0	24,375	22,598,431	100,860	-26.3	34,000	The minimum amount of time a bank must stay active (ACT to PRE(A)) must meet tPACT.
37	21,624	h/ACT Time	21,624	21,624	0	23,279	22,598,431	100,860	-100.0	70,200,000	The minimum amount of time a bank can stay active (ACT to PRE(A)) must meet tPACT.
38	0	ACT to RDAA/WRRA	0	0	0	NA	NA	NA	NA	3,600	Minimum time from a activate (ACT) command to a read (RDAA) or write (WRRA) command must meet tARW.
39	0	RD to PRE(A)	0	0	0	6,679	128,672	10,282	-27.1	9,162	The minimum amount of time from a read (RD) command to a precharge (PRE(A)) command must meet tRPP.
40	0	RD to REF	0	0	0	6,679	128,672	10,282	-27.1	9,162	The minimum amount of time from a read (RD) command to a refresh (REF) command must meet tRPP.
41	10,107	WR to PRE(A)	10,107	10,107	0	26,290	246,390	19,846	-21.1	31,200	The minimum amount of time from a write (WR) command to a precharge (PRE(A)) command must meet tRPP.
42	0	WR to ACT	0	0	0	26,290	246,390	19,846	-21.1	27,485	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet tRPP.
43	237	0	237	0	0	35,175	6,592,414	271,847	105.8	13,254	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet tRPP.
44	0	CHX Signal After DLL Reset	0	0	0	NA	NA	NA	NA	501,070	Rank CHX must remain high GCLK wire after a DLL Reset.

Figure 11 - Detailed Compliance Analysis Results



Figure 12 - View Violations in Data Across Many Acquisitions

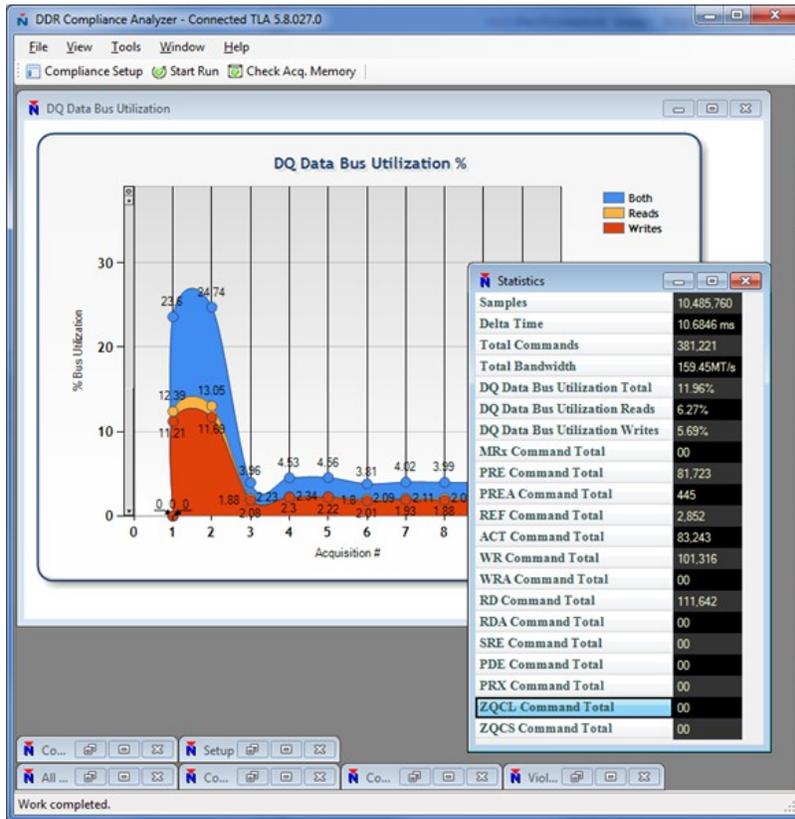


Figure 13 - Bus Utilization Measurements

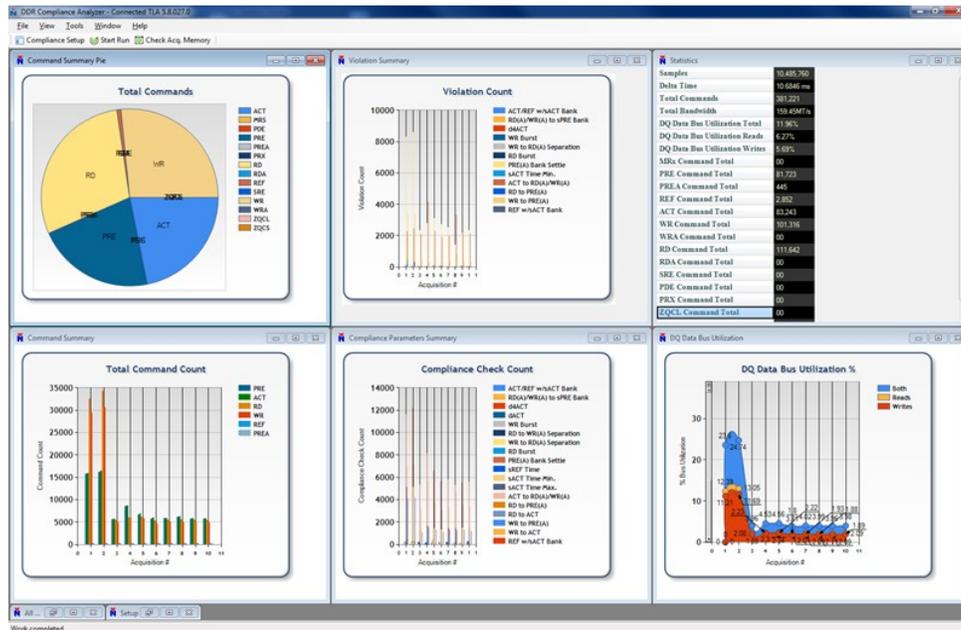


Figure 14 - Graphical and Tabular Compliance Analysis Examples

Nexus Technology LPDDR3 Component Interposer Advantages

Probed at the BGA Pads

The best place to probe a memory bus is at the BGA balls to eliminate reflections associated with break-out board probing, embedded mid-bus probing or other methods. Nexus Technology's component interposers provide easy access to memory component BGA pads for accurate memory bus analysis.

Use with Existing Package-on-Package or Embedded designs

No need to change existing designs. Simply add the interposer to your embedded target or DIMM with no re-design or added probe points. No Need to add probe points to existing designs. Simply add the interposer to your DIMM or embedded target for easy connectivity to the Logic Analyzer.

Interchangeable Socketed Interposers

The interposers are reusable. Once an interposer socket is installed on a target, the interposer can be attached and removed by hand. This allows an interposer to be used on multiple targets, or enables quick swapping of logic analyzer and oscilloscope interposers on the same target. The interposer socket has four posts that are soldered to four mounting holes on the interposer to retain the interposer to the socket

Easy to Install

Install the interposer socket using industry standard BGA Attachment methods or by using Nexus Technology's Attachment Service. Contact Nexus Technology for further information on our Attachment Service.

Simple Digital and Analog Validation via Standard Interposer Socket

Nexus Technology's Component interposers are designed for optimal signal integrity. Once our custom socket is installed on your target, our interposers can be easily swapped out. We offer Oscilloscope component interposers for analog validation, and Logic Analyzer component interposers for digital validation.

Product Dimensions

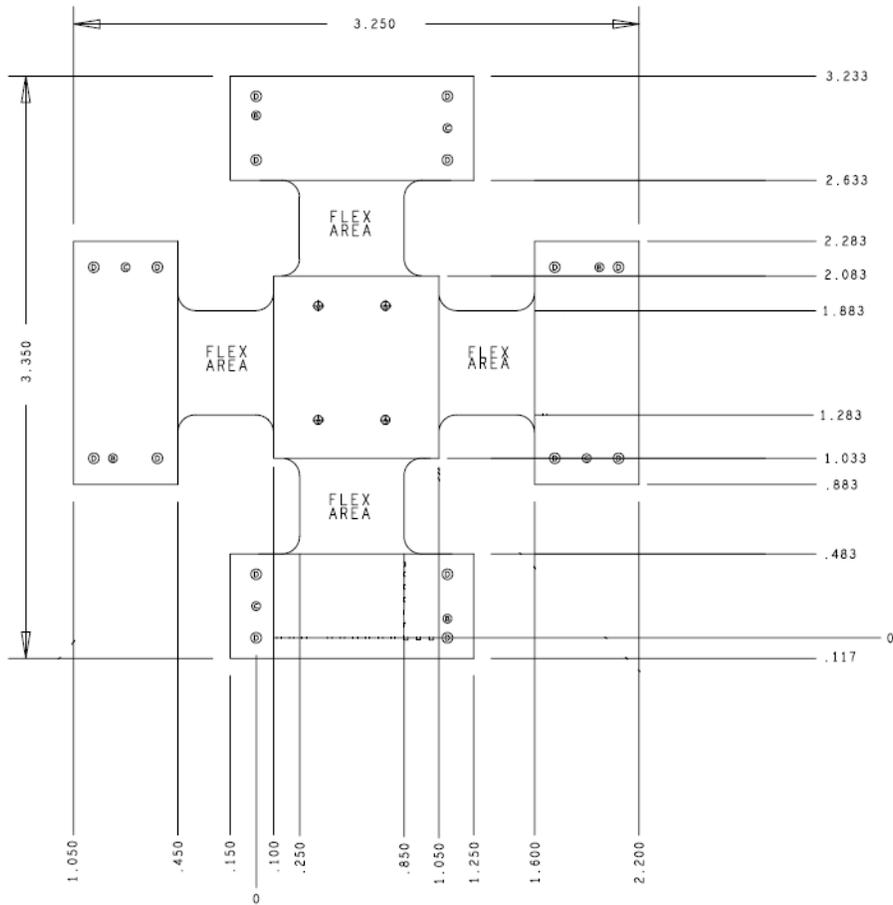
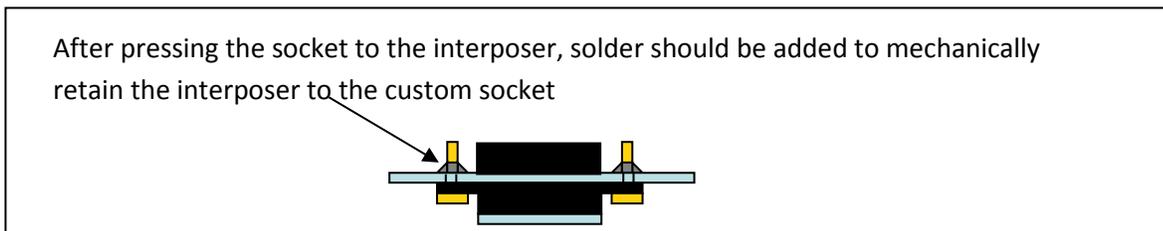
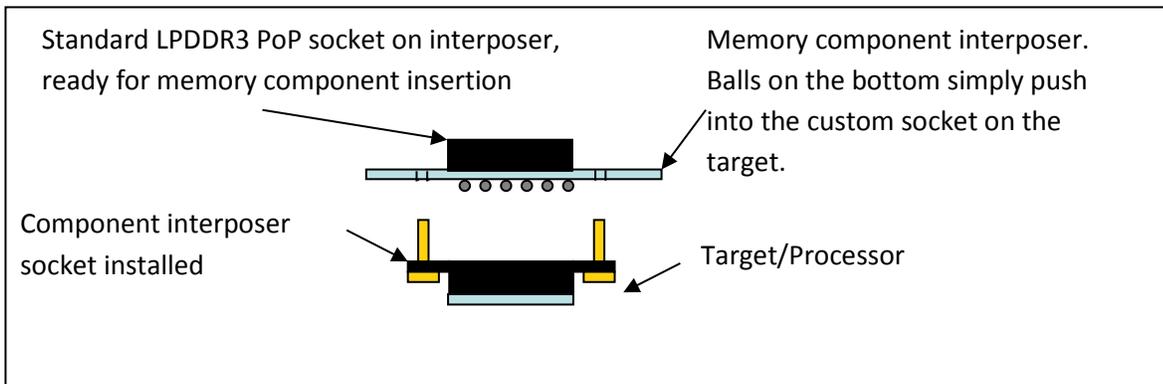


Figure 15 - LPDDR3 216 – ball /4Logic Analyzer Component Interposer Dimensions

Attaching and Reusing Interposers



LPDDR3 PoP 216 Ball Logic Analyzer Component Interposer

Configuration Tables

LPDDR3 PoP 216 Ball Logic Analyzer Interposers

Nomenclature	Interposer Type	Data Width	Component Socket Included	Nexus Probes Included	Installation Service Included	Hardware Requirements
NEX-LPDDR3PoP216BLASK	Logic Analyzer	2x32	Yes	No ¹	No	1- TLA7000 Series Mainframe 1- TLA7Bx4 1.4 GHz Acquisition Card Call Nexus for accurate probe requirements
NEX-LPDDR3PoP216BLASK-AT	Logic Analyzer	2x32	Yes	No ¹	Yes	
NEX-LPDDR3PoP216BLASKPR	Logic Analyzer	2x32	Yes	Yes ¹	No	
NEX-LPDDR3PoP216BLASKPR-AT	Logic Analyzer	2x32	Yes	Yes ¹	Yes	

Optional Additional LPDDR3 PoP 216 Ball Interposer Sockets

Nomenclature	Solder Balls Added	Quantity of Sockets
NEX-LP3-216BGASKBA	Yes	1
NEX-LP3-216BGASKBA-3	Yes	3

Product Support

Product Support is critical to your success. Our engineering staff can provide expert training and support tailored to your specific needs. Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

Telephone 877-595-8116

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Fax 877-595-8118

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