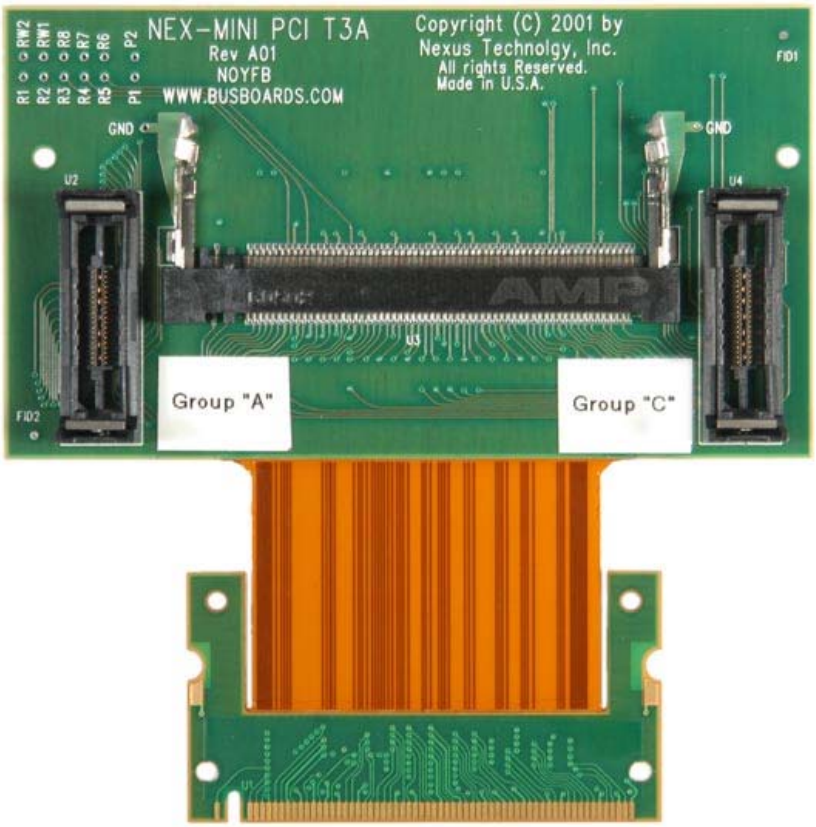
Mini-PCI Type 3A Bus Adapter and Analysis Software for Tektronix Logic Analyzers

NEX-MINIPCIT3A



- Rigid/Flex/Rigid design provides mechanical clearance for use in standard MiniPCI Type 3A targets.
- High Density connectors provide quick convenient connection to the MiniPCI bus
- Disassembly of the MiniPCI Bus
  - Cycle Identification
  - Config Cycle decoding including register evaluation
  - Ability to selectively ignore Idle and Wait States
- Extender card design
- Logic Analyzer Setup Software gets you up and running fast
- Simultaneous State and Timing acquisition on each channel
- Trigger on setup/hold violations on all channels

Please contact us for information on other PCI adapters including: a PCI 32/64-bit card.

General Description

Mini-PCI Disassembly Software

The included NEX-MINIPCI disassembly software executes on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All Mini-PCI Cycle types are identified and Config cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state presented in easy-to-read text (see Fig. 1). Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE disk, Video controller, network interface, etc.) is being accessed (see Fig. 1).

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest. Figure 4 shows the same area of acquired data as that in Figure 1, but with Memory and I/O cycles suppressed

Another feature of the disassembly software is its ability to intelligently acquire Mini-PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the Mini-PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and acquire data on every Mini-PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

Timing analysis of the Mini-PCI bus can be done at the maximum asynchronous rate of the Tektronix Logic Analyzer. For example a TLA700/600 system with a minimum of 102 channel acquisition module can acquire timing data at 8GHz (125ps) on each channel. Fast timing acquisition and low capacitive loading (the passive NEX-MINIPCIT3A adapter module and the < 2pf/P6434 and 0.7pf/P6860 logic analyzer probe) provide excellent timing analysis on each monitored channel of the Mini-PCI bus.

NEX-MINIPCIT3A Adapter Module

The NEX-MINIPCIT3A adapter provides a quick convenient connection to standard Tektronix logic analyzers. It requires the use of two Tektronix P6434/P6860 high density probes for connection to the TLA700/600.

The NEX-MINIPICT3A extends the Mini-PCI bus. Depending on the design of the system, users may experience difficulties with this. The Logic Analyzer attaches to the NEX-MINIPCIT3A adapter using a high density, impedance matched connector. The typical Logic Analyzer loading is < 2 pf/P6434 and 0.7pf/P6860.

Timestamp

All acquired data is timestamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this. The timestamp resolution on the TLA700/600 system is 125ps.

Correlation

While the NEX-MINICIT3A package is being used with a Tektronix logic analyzer to monitor the Mini-PCI activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and Mini-PCI bus communication.

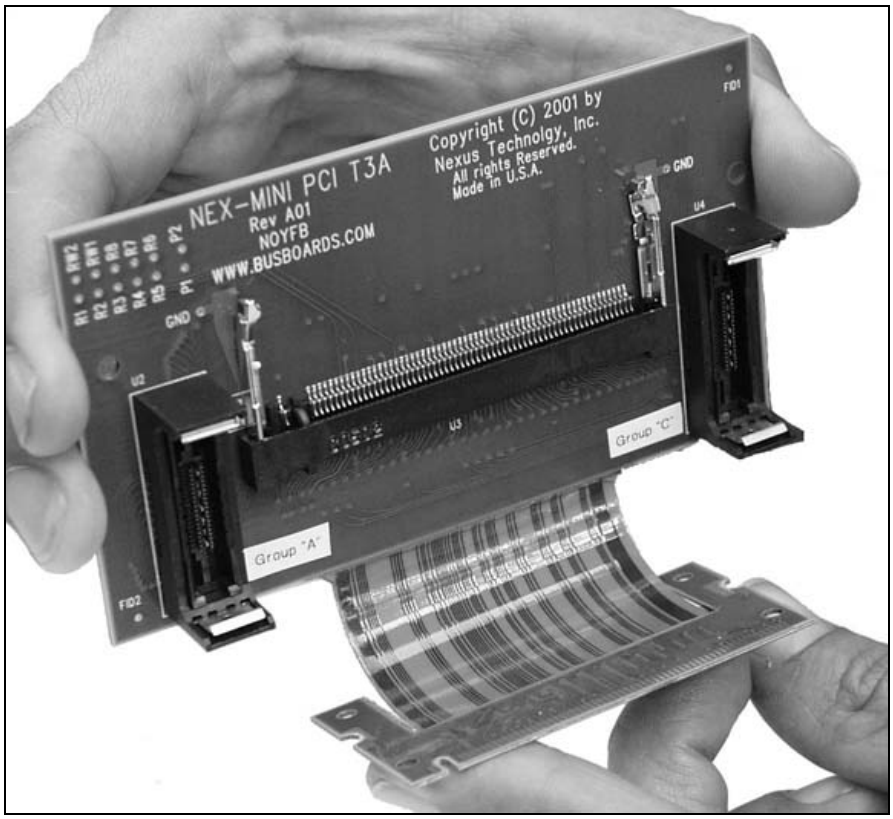
Setup/Hold Triggering

Setup and hold specifications can be verified and margins tested using the TLA700/600. Each channel group (address, data, control, etc…) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or any channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation. The timing resolution of the acquired data at the violation point is 8GHz (125ps).

Setup and hold margin testing can be done by altering the setup and hold times set for the violation trigger in 125ps increments. Changing these values until a violation occurs will show the actual setup and hold of the system under test.

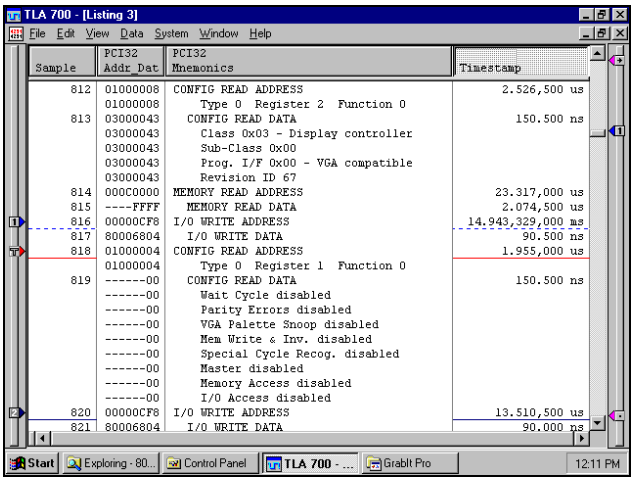
Simultaneous State and Timing Acquisition

The Tektronix TLA700/600 Logic Analyzer offers the capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-MINIPCIT3A custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.



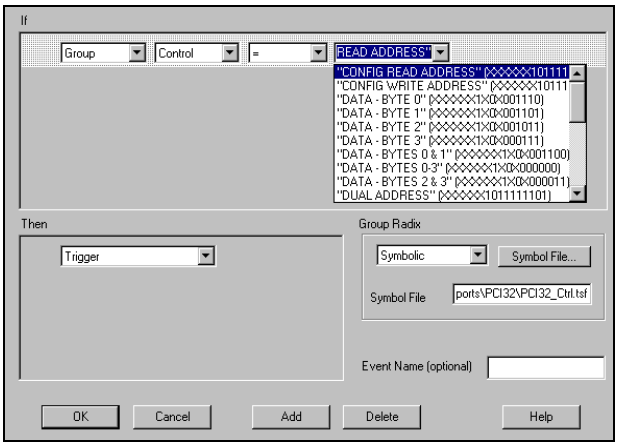
The NEX-MINIPCIT3A is a rigid/flex/rigid design that allows for the mechanical clearance necessary to connect to the target.

Disassembly (State Analysis)



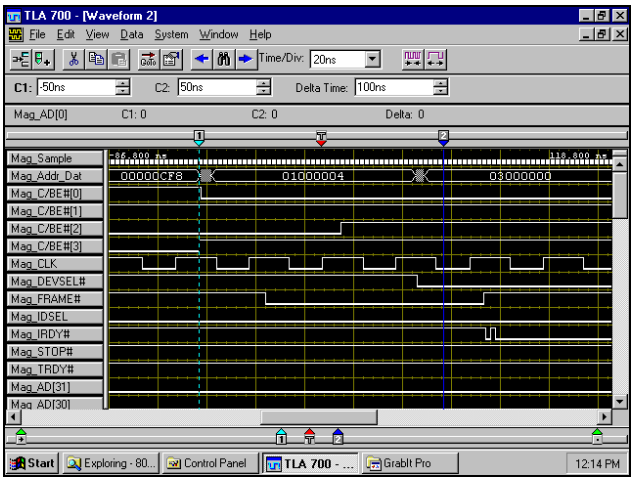
Mini-PCI cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class and Type.

Triggering



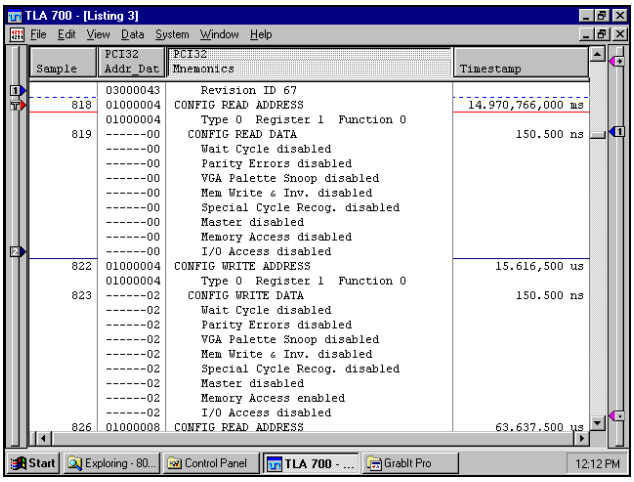
Trigger on pre-defined Mini-PCI cycles

Timing Analysis



125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate Mini-PCI signal name. Bus format display of grouped signals shown.

Disassembly (with Data Filtering)

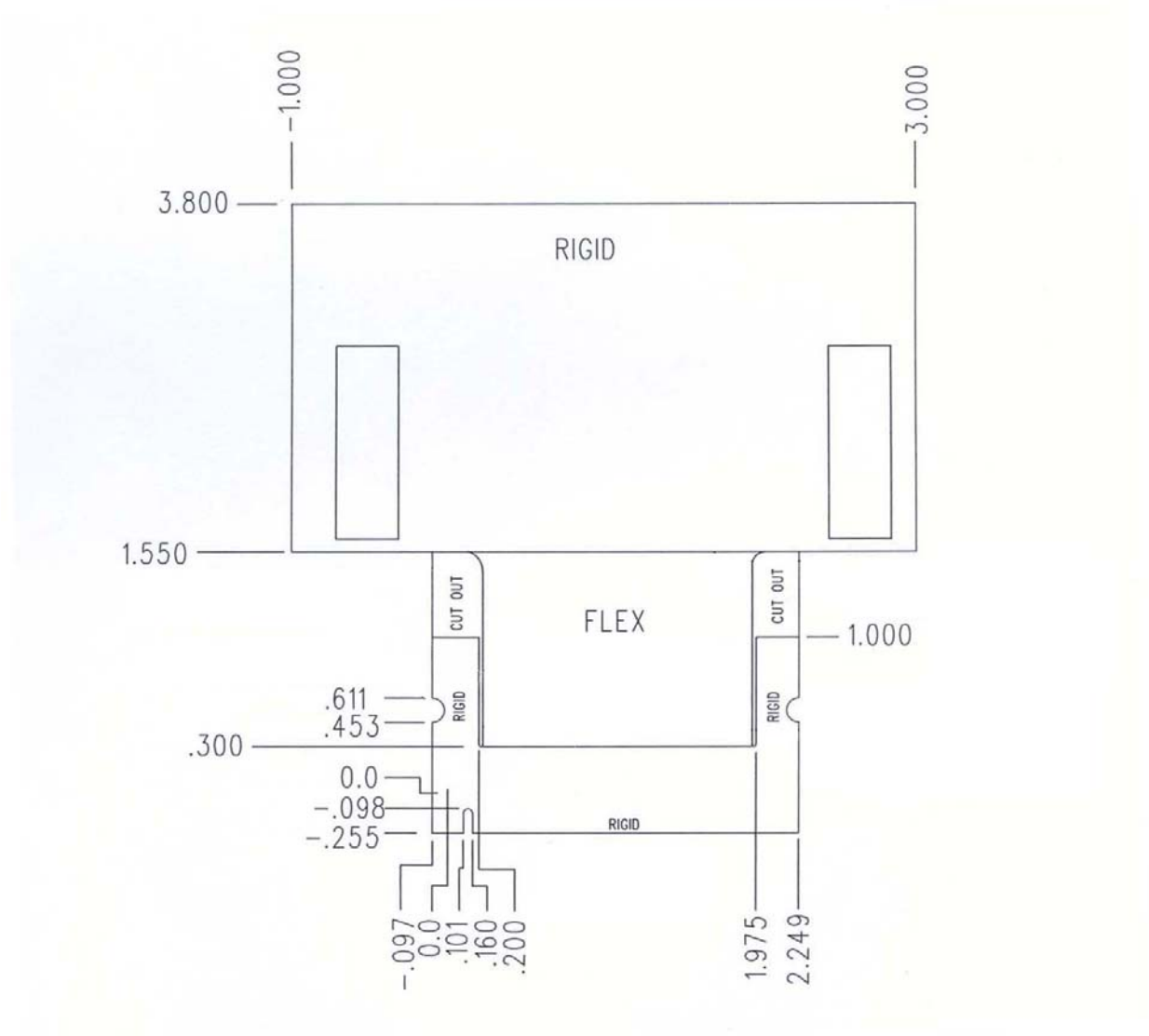


Same disassembly display as Figure 1 but with Memory and I/O cycles suppressed.

Tektronix Logic Analyzers Supported

TLA600 or TLA700 with a minimum of 102 channel acquisition module.
Requires 2-P6434/P6860 probes from Tektronix.

Mechanical Outline



Ordering / Contact Information

Part Number NEX-MINIPCIT3A
Includes: NEX-MINIPCI Type 3A Bus Adapter
Software
Manual

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.