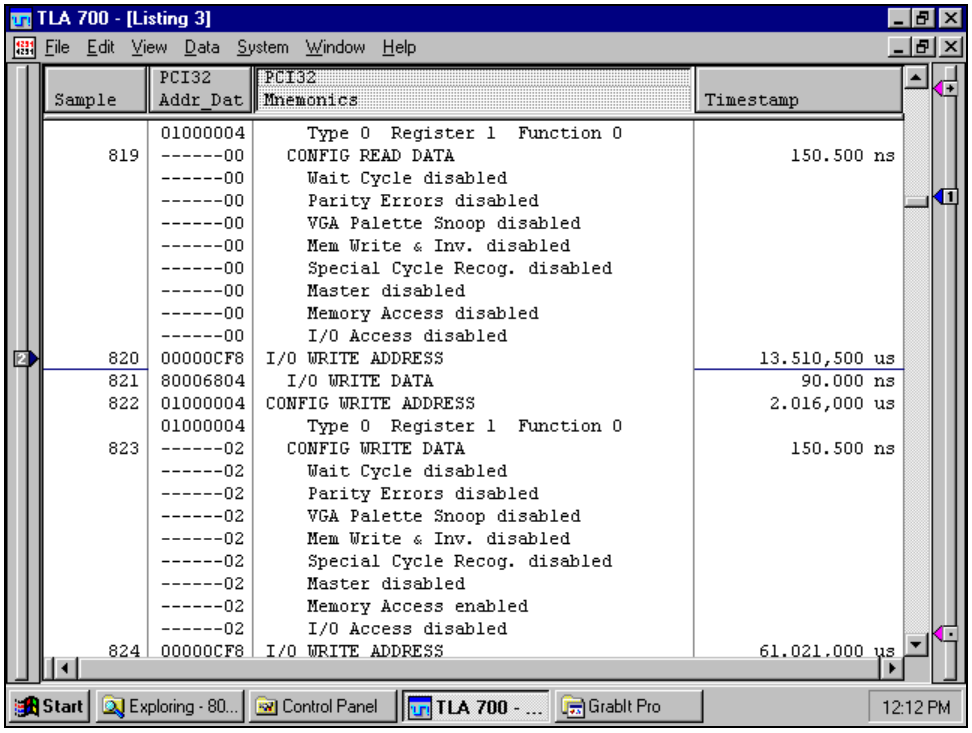
NEXUS TECHNOLOGY

PCI 32-bit and 64-bit Analysis Software for Tektronix Logic Analyzer

NEX-PCI32SWL & NEX-PCI3264SWL



- Disassembly of the PCI Bus
  - Cycle Identification
  - Config Cycle decoding including register evaluation
  - Ability to selectively ignore Idle and Wait States
- Timing Analysis to 8GHz (125ps) on each Channel
- Logic Analyzer Setup S/W gets you up and running fast
- Simultaneous State and Timing Acquisition on each Channel *
- Trigger on setup/hold violations on all Channels *

Please contact us for information on our PCI adapters including: a PCI 32 or 64-bit extender card, PCI 32-bit short card, and a PCI 32/64-bit card.

General Description

Connecting to a Target / PCI Adapter Modules

The NEX-PCI32SWL and NEX-PCI3264SWL product is software only. It is intended to be used when connectors (typically Mictors) are designed into a target. Please refer to the Manual for the NEX-PCI32SWL or NEX-PCI3264SWL for more information.

The software can also be used with an interface adapter (not included). Please call for information on products that include a PCI bus adapter with PCI disassembly software.

Disassembly Software

The disassembly software executes on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All PCI Cycle types are identified and Config cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text (see Fig. 1). Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE disk, Video controller, network interface, etc.) is being accessed (see Fig. 1).

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest. Figure 4 shows the same area of acquired data as that in Figure 1, but with Memory and I/O cycles suppressed

Another feature of the disassembly software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

Timing analysis of the PCI bus can be done at the maximum asynchronous rate of the Tektronix Logic Analyzer. For example the TLA600/700 system can acquire timing data at 8GHz (125ps) on each channel. Fast timing acquisition and low capacitive loading (< 2pf/P6434 and 0.7pf/P6860 logic analyzer probe) provide excellent timing analysis on each monitored channel of the PCI bus.

Timestamp

All acquired data is timestamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this. The timestamp resolution on the TLA600/700 system is 125ps, and 10ns on the DAS9200 and TLA510/20.

Correlation

While the PCI disassembly software is being used to monitor the PCI activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and PCI bus communication.

Setup/Hold Triggering

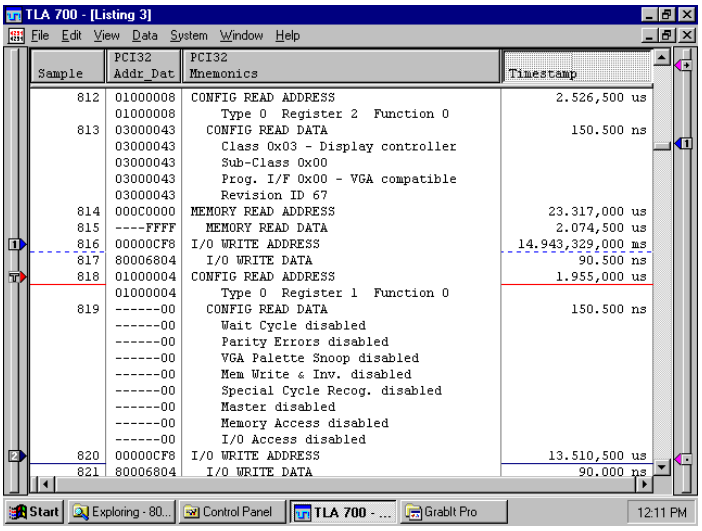
Setup and hold specifications can be verified, and margins tested, using the TLA600/700 system. Each channel group (address, data, control, etc..) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or any channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation. The timing resolution of the acquired data at the violation point is 8GHz (125ps).

Setup and hold margin testing can be done by altering the setup and hold times set for the violation trigger in 125ps increments. Changing these values until a violation occurs will show the actual setup and hold of the system under test.

Simultaneous State and Timing Acquisition

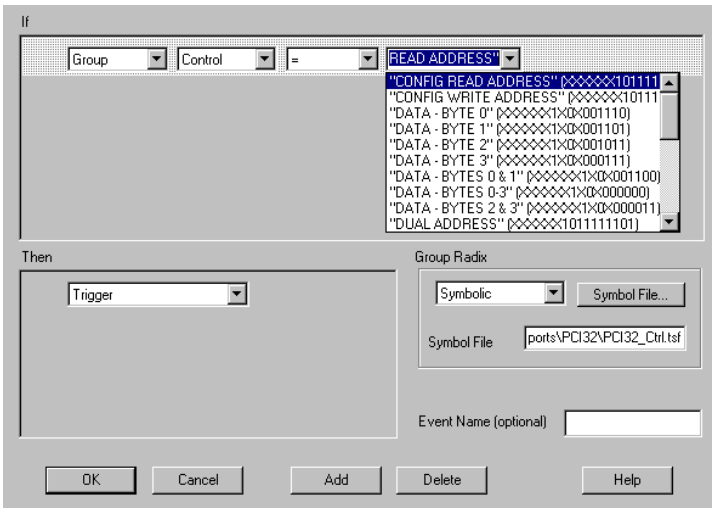
The Tektronix TLA600/700 Logic Analyzer offers the unique capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-PCI32SWL custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.

Disassembly (State Analysis)



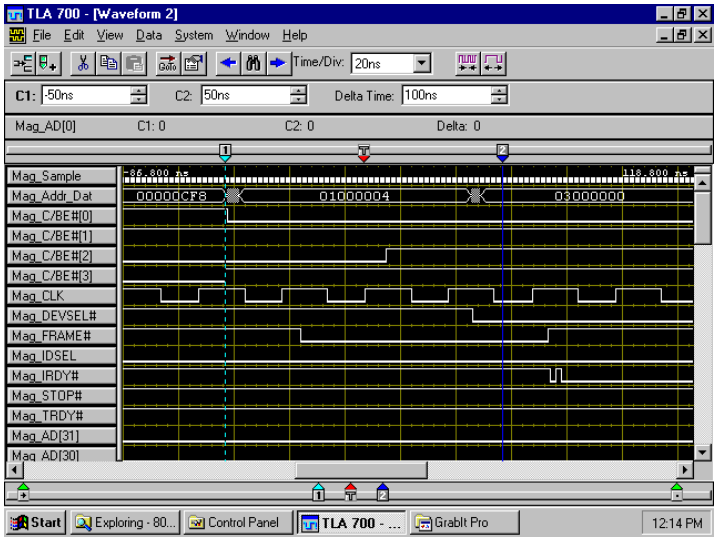
PCI cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class, and Type.

Triggering



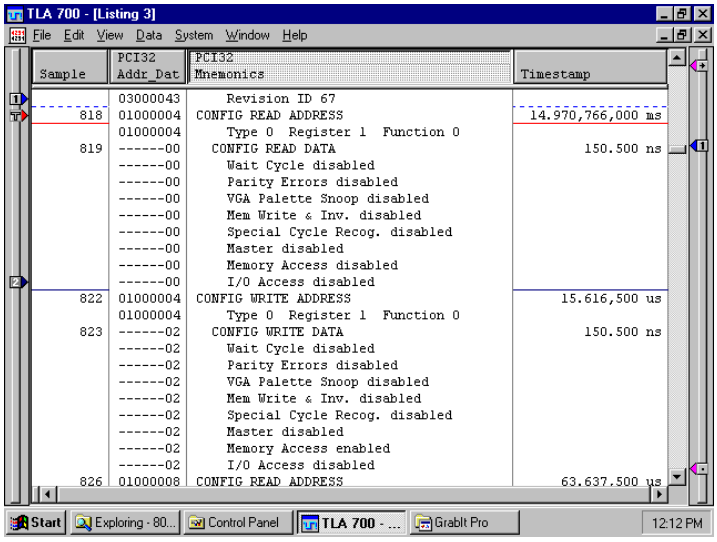
Trigger on pre-defined PCI cycles

Timing Analysis



125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate PCI signal name. Bus format display of grouped signals shown.

Disassembly (with Data Filtering)



Same disassembly display with Memory and I/O cycles supressed.

PCI 32-bit Mictor Pinout

The following Mictor wiring must be followed if the NEX-PCI32L or NEX-PCI32L68 disassembly software is to be used. Please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual or the P6860 Logic Analyzer Probe Manual for further information on designing the Mictor connectors into your target. TLA inputs that show dashes ('---') in the PCI Signal and Pin Number columns are unassigned, and may be connected to any target signal desired.

C/BE[0]#, C/BE[1]#, C/BE[2]# and C/BE[3]# are double probed. This is required to support de-muxing the PCI address/data group for 32-bit PCI support. If 32-bit demux is not desired or if the additional loading is a concern, the following signals may be left unconnected.

PCI Signal Name	TLA700 Pin
C/BE[0]#	C1:4
C/BE[1]#	C1:5
C/BE[2]#	C1:6
C/BE[3]#	C1:7

Tek Mictor Pin #	**AMP Mictor Pin #**	**TLA700 Channel**	**PCI Signal Name**	**PCI Pin #**	**Tek Mictor Pin #**	**AMP Mictor Pin #**	**TLA700 Channel**	**PCI Signal Name**	**PCI Pin #**
3	5	CLK:0	---	---	36	6	CLK:1	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[1]	B58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[0]	A58

Mictor Group A

Note:
All signals on this Mictor required for proper clocking and disassembly

Tek **Mictor Pin #**	**AMP Mictor Pin #**	**TLA700 Channel**	**PCI Signal Name**	**PCI Pin #**	**Tek Mictor Pin #**	**AMP Mictor Pin #**	**TLA700 Channel**	**PCI Signal Name**	**PCI Pin #**
3	5	CLK:3[2]	CLK	B16	36	6	QUAL:1	---	---
4	7	---	---	B16	35	8	C1:7[3]	C/BE[3]#	B26
5	9	C3:6	SDONE	A40	34	10	C1:6[3]	C/BE[2]#	B33
6	11	C3:5	RST#	A15	33	12	C1:5[3]	C/BE[1]#	B44
7	13	C3:4	LOCK#	B39	32	14	C1:4[3]	C/BE[0]#	A52
8	15	C3:3	PERR#	B40	31	16	C1:3	SBO#	A41
9	17	C3:2	PAR	A43	30	18	C1:2	---	---
10	19	C3:1	SERR#	B42	29	20	C1:1	ACQ64#	B60
11	21	---	---	B37	28	22	C1:0	REQ64#	A60
12	23	C2:7[1,2]	C/BE[3]#	B26	27	24	C0:7	M66EN	B49
13	25	C2:6[1,2]	C/BE[2]#	B33	26	26	C0:6	GNT#	A17
14	27	C2:5[1,2]	C/BE[1]#	B44	25	28	C0:5	REQ#	B18
15	29	C2:4[1,2]	C/BE[0]#	A52	24	30	C0:4	IDSEL	A26
16	31	C2:3[2]	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:2[2]	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:1[2]	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:0[2]	FRAME#	A34	20	38	C0:0	INTA#	A06

Group C Mictor

Notes:
C/BE[3-0]# are also connected to C1:7-4.
These signals are required for proper 32-bit clocking and disassembly.
These signals may be left unconnected if 32-bit de-mux is not desired.

PCI 32-bit Compression Pinout

Pad P3-PH2	Input	PCI Signal Name	PCI Pin #
A15	CK0-		
A13	CK0+		
B12	A3:7	AD[31]	B20
B10	A3:6	AD[30]	A20
A12	A3:5	AD[29]	B21
A10	A3:4	AD[28]	A22
B9	A3:3	AD[27]	B23
B7	A3:2	AD[26]	A23
A9	A3:1	AD[25]	B24
A7	A3:0	AD[24]	A25
B6	A2:7	AD[23]	B27
B4	A2:6	AD[22]	A28
A6	A2:5	AD[21]	B29
A4	A2:4	AD[20]	A29
B3	A2:3	AD[19]	B30
B1	A2:2	AD[18]	A31
A3	A2:1	AD[17]	B32
A1	A2:0	AD[16]	A32

Pad P2-PH2	Input	PCI Signal Name	PCI Pin #
A15	CK1-	Gnd	Gnd
A13	CK1+	DEVSEL#	B37
B12	A1:7	AD[15]	A44
B10	A1:6	AD[14]	B45
A12	A1:5	AD[13]	A46
A10	A1:4	AD[12]	B47
B9	A1:3	AD[11]	A47
B7	A1:2	AD[10]	B48
A9	A1:1	AD[9]	A49
A7	A1:0	AD[8]	B52
B6	A0:7	AD[7]	B53
B4	A0:6	AD[6]	A54
A6	A0:5	AD[5]	B55
A4	A0:4	AD[4]	A55
B3	A0:3	AD[3]	B56
B1	A0:2	AD[2]	A57
A3	A0:1	AD[1]	B58
A1	A0:0	AD[0]	A58

Pad P1-PH2	Input	PCI Signal Name	PCI Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	CLK	B16
B12	C3:7		
B10	C3:6	SDONE	A40
A12	C3:5	RST#	A15
A10	C3:4	LOCK#	B39
B9	C3:3	PERR#	B40
B7	C3:2	PAR	A43
A9	C3:1	SERR#	B42
A7	C3:0	---	B37
B6	C2:7	C/BE[3]#	B26
B4	C2:6	C/BE[2]#	B33
A6	C2:5	C/BE[1]#	B44
A4	C2:4	C/BE[0]#	A52
B3	C2:3	STOP#	A38
B1	C2:2	TRDY#	A36
A3	C2:1	IRDY#	B35
A1	C2:0	FRAME#	A34

Pad P1-PH1	Input	PCI Signal Name	PCI Pin #
A15	Q1-		
A13	Q1+		
B12	C1:7	C/BE[3]#	B26
B10	C1:6	C/BE[2]#	B33
A12	C1:5	C/BE[1]#	B44
A10	C1:4	C/BE[0]#	A52
B9	C1:3	SBO#	A41
B7	C1:2	---	---
A9	C1:1	ACQ64#	B60
A7	C1:0	REQ64#	A60
B6	C0:7	M66EN	B49
B4	C0:6	GNT#	A17
A6	C0:5	REQ#	B18
A4	C0:4	IDSEL	A26
B3	C0:3	INTD#	B08
B1	C0:2	INTC#	A07
A3	C0:1	INTB#	B07
A1	C0:0	INTA#	A06

PCI 32/64-bit Mictor Pinout

The following Mictor wiring must be followed if the NEX-PCI64L disassembly software is to be used. Please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual for further information on designing the Mictor connectors into your target. TLA inputs that show dashes ('---') in the PCI Signal and Pin Number columns are unassigned, and may be connected to any target signal desired.

C/BE[0]#, C/BE[1]#, C/BE[2]# and C/BE[3]# are double probed. This is required to support de-muxing the PCI address/data group for 32-bit PCI support. If 32-bit demux is not desired or if the additional loading is a concern, the following signals may be left unconnected.

PCI Signal Name	TLA700 Pin
C/BE[0]#	C1:4
C/BE[1]#	C1:5
C/BE[2]#	C1:6
C/BE[3]#	C1:7

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	PCI Signal Name	PCI Pin #
3	5	CLK:0[2]	C/BE[3]#	B26	36	6	CLK:1	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[1]	B58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[0]	A58

Group A Mictor

Notes:
All signals on this Mictor required for proper 32- or 64-bit clocking and disassembly.
These signals may be left unconnected if 32-bit de-mux is not desired.

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	PCI Signal Name	PCI Pin #
3	5	CLK:31	CLK	B16	36	6	QUAL:13	C/BE[0]#	A52
4	7	---	---	B16	35	8	C1:72	C/BE[7]#	A64
5	9	C3:6	SDONE	A40	34	10	C1:62	C/BE[6]#	B65
6	11	C3:51	RST#	A15	33	12	C1:52	C/BE[5]#	A65
7	13	C3:4	LOCK#	B39	32	14	C1:42	C/BE[4]#	B66
8	15	C3:3	PERR#	B40	31	16	C1:3	SBO#	A41
9	17	C3:2	PAR	A43	30	18	C1:2	PAR64	A67
10	19	C3:1	SERR#	B42	29	20	C1:12	ACQ64#	B60
11	21	---	---	B37	28	22	C1:02	REQ64#	A60
12	23	C2:71	C/BE[3]#	B26	27	24	C0:7	M66EN	B49
13	25	C2:61	C/BE[2]#	B33	26	26	C0:6	GNT#	A17
14	27	C2:51	C/BE[1]#	B44	25	28	C0:5	REQ#	B18
15	29	C2:41	C/BE[0]#	A52	24	30	C0:4	IDSEL	A26
16	31	C2:31	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:21	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:11	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:01	FRAME#	A34	20	38	C0:0	INTA#	A06

Group C Mictor

Notes:
These signals are required for proper 32- or 64-bit clocking and disassembly
These signals are required for proper 64-bit disassembly
These signals may be left unconnected if 32-bit de-mux is not desired.

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	PCI Signal Name	PCI Pin #
3	5	QUAL:02	C/BE[1]#	B44	36	6	CLK:22	C/BE[2]#	B33
4	7	D3:7	AD[63]	B68	35	8	D1:7	AD[47]	B80
5	9	D3:6	AD[62]	A68	34	10	D1:6	AD[46]	A80
6	11	D3:5	AD[61]	B69	33	12	D1:5	AD[45]	B81
7	13	D3:4	AD[60]	A70	32	14	D1:4	AD[44]	A82
8	15	D3:3	AD[59]	B71	31	16	D1:3	AD[43]	B83
9	17	D3:2	AD[58]	A71	30	18	D1:2	AD[42]	A83
10	19	D3:1	AD[57]	B72	29	20	D1:1	AD[41]	B84
11	21	D3:0	AD[56]	A73	28	22	D1:0	AD[40]	A85
12	23	D2:7	AD[55]	B74	27	24	D0:7	AD[39]	B86
13	25	D2:6	AD[54]	A74	26	26	D0:6	AD[38]	A86
14	27	D2:5	AD[53]	B75	25	28	D0:5	AD[37]	B87
15	29	D2:4	AD[52]	A76	24	30	D0:4	AD[36]	A88
16	31	D2:3	AD[51]	B77	23	32	D0:3	AD[35]	B89
17	33	D2:2	AD[50]	A77	22	34	D0:2	AD[34]	A89
18	35	D2:1	AD[49]	B78	21	36	D0:1	AD[33]	B90
19	37	D2:0	AD[48]	A79	20	38	D0:0	AD[32]	A91

Group D Mictor

Notes:
All signals on this Mictor required for proper 64-bit disassembly.
These signals may be left unconnected if 32-bit de-mux is not desired.

PCI 32/64-bit Compression Pinout

Pad P3-PH2	Input	PCI Signal Name	PCI Pin #
A15	CK0-	Gnd	Gnd
A13	CK0+	C/BE[3]#	B26
B12	A3:7	AD[31]	B20
B10	A3:6	AD[30]	A20
A12	A3:5	AD[29]	B21
A10	A3:4	AD[28]	A22
B9	A3:3	AD[27]	B23
B7	A3:2	AD[26]	A23
A9	A3:1	AD[25]	B24
A7	A3:0	AD[24]	A25
B6	A2:7	AD[23]	B27
B4	A2:6	AD[22]	A28
A6	A2:5	AD[21]	B29
A4	A2:4	AD[20]	A29
B3	A2:3	AD[19]	B30
B1	A2:2	AD[18]	A31
A3	A2:1	AD[17]	B32
A1	A2:0	AD[16]	A32

Pad P3-PH1	Input	PCI Signal Name	PCI Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+	C/BE[1]#	B44
B12	D3:7	AD[63]	B68
B10	D3:6	AD[62]	A68
A12	D3:5	AD[61]	B69
A10	D3:4	AD[60]	A70
B9	D3:3	AD[59]	B71
B7	D3:2	AD[58]	A71
A9	D3:1	AD[57]	B72
A7	D3:0	AD[56]	A73
B6	D2:7	AD[55]	B74
B4	D2:6	AD[54]	A74
A6	D2:5	AD[53]	B75
A4	D2:4	AD[52]	A76
B3	D2:3	AD[51]	B77
B1	D2:2	AD[50]	A77
A3	D2:1	AD[49]	B78
A1	D2:0	AD[48]	A79

Pad P2-PH2	Input	PCI Signal Name	PCI Pin #
A15	CK1-	Gnd	Gnd
A13	CK1+	DEVSEL#	B37
B12	A1:7	AD[15]	A44
B10	A1:6	AD[14]	B45
A12	A1:5	AD[13]	A46
A10	A1:4	AD[12]	B47
B9	A1:3	AD[11]	A47
B7	A1:2	AD[10]	B48
A9	A1:1	AD[9]	A49
A7	A1:0	AD[8]	B52
B6	A0:7	AD[7]	B53
B4	A0:6	AD[6]	A54
A6	A0:5	AD[5]	B55
A4	A0:4	AD[4]	A55
B3	A0:3	AD[3]	B56
B1	A0:2	AD[2]	A57
A3	A0:1	AD[1]	B58
A1	A0:0	AD[0]	A58

Pad P2-PH1	Input	PCI Signal Name	PCI Pin #
A15	CK2-	Gnd	Gnd
A13	CK2+	C/BE[2]#	B33
B12	D1:7	AD[47]	B80
B10	D1:6	AD[46]	A80
A12	D1:5	AD[45]	B81
A10	D1:4	AD[44]	A82
B9	D1:3	AD[43]	B83
B7	D1:2	AD[42]	A83
A9	D1:1	AD[41]	B84
A7	D1:0	AD[40]	A85
B6	D0:7	AD[39]	B86
B4	D0:6	AD[38]	A86
A6	D0:5	AD[37]	B87
A4	D0:4	AD[36]	A88
B3	D0:3	AD[35]	B89
B1	D0:2	AD[34]	A89
A3	D0:1	AD[33]	B90
A1	D0:0	AD[32]	A91

Pad P1-PH2	Input	PCI Signal Name	PCI Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	CLK	B16
B12	C3:7		
B10	C3:6	SDONE	A40
A12	C3:5	RST#	A15
A10	C3:4	LOCK#	B39
B9	C3:3	PERR#	B40
B7	C3:2	PAR	A43
A9	C3:1	SERR#	B42
A7	C3:0	---	B37
B6	C2:7	C/BE[3]#	B26
B4	C2:6	C/BE[2]#	B33
A6	C2:5	C/BE[1]#	B44
A4	C2:4	C/BE[0]#	A52
B3	C2:3	STOP#	A38
B1	C2:2	TRDY#	A36
A3	C2:1	IRDY#	B35
A1	C2:0	FRAME#	A34

Pad P1-PH1	Input	PCI Signal Name	PCI Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+	C/BE[0]#	A52
B12	C1:7	C/BE[7]#	A64
B10	C1:6	C/BE[6]#	B65
A12	C1:5	C/BE[5]#	A65
A10	C1:4	C/BE[4]#	B66
B9	C1:3	SBO#	A41
B7	C1:2	PAR64	A67
A9	C1:1	ACQ64#	B60
A7	C1:0	REQ64#	A60
B6	C0:7	M66EN	B49
B4	C0:6	GNT#	A17
A6	C0:5	REQ#	B18
A4	C0:4	IDSEL	A26
B3	C0:3	INTD#	B08
B1	C0:2	INTC#	A07
A3	C0:1	INTB#	B07
A1	C0:0	INTA#	A06

Tektronix Logic Analyzers Supported

TLA600 or 700
For 32-bit and 64-bit PCI support, you will need a minimum of 102 channel acquisition module. 32-bit PCI support only using special included NEX-PCI32L68 software TLA510 or TLA520 (one acquisition module used)
DAS9200 with a 92A96 or 92C96 (any memory depth)

Ordering / Contact Information

Part Number NEX-PCI32SWL: Single User License for 32-bit PCI Bus Analysis Software
Includes: Manual
NEX-PCI32L: 32-bit PCI analysis Software for TLA600/700 with 102 or 136 channel acquisition module
DAS9200 with/92A96, TLA510/520 3 1/2" floppy
NEX-PCI32L68: 32-bit PCI analysis Software for TLA600/700 with 68 channel acquisition module

Part Number NEX-PCI32SWL/5: Five User License for 32-bit PCI Bus Analysis Software
Includes: Same as NEX-PCI32SWL above

Part Number NEX-PCI3264SWL: Single User License for 32 and 64-bit PCI Bus Analysis Software
Includes: Same as NEX-PCI32SWL and adds:
NEX-PCI64L: 64-bit PCI analysis Software for TLA704/711 with 102 or 136 channel acquisition module
DAS9200 with/92A96, TLA510/520 3 1/2" floppy

Part Number NEX-PCI3264SWL/5: Five User License for 32 and 64-bit PCI Bus Analysis Software
Includes: Same as NEX-PCI3264SWL above

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