NEXUS TECHNOLOGY

PCI 32/64-bit Interposer & Analysis Software for Tektronix Logic Analyzers

NEX-PCIINTR

- Quick & convenient connection to the PCI bus
- Disassembly of PCI bus transactions
- Straddle mount PCI Connector
- Narrow keep-out with right angle probe connections
- Uses P6960 probes
- Controlled impedance design
- Matched signal length design
- No active buffering of the PCI signals
- Designed for 66MHz+ PCI
- Timing analysis to 8 GS/s (125ps) on every channel
- Oscilloscope connectivity to any channel without having to re-probe via the TLA's Enhanced iView Analog Mux capability.
- Logic analyzer Setup Software gets you up and running fast
- Simultaneous state and timing acquisition on each channel
- Trigger on Setup/Hold violations on all channels

General Description

NEX-PCIINTR was designed for 32- and 64-bit PCI, 3V or 5V applications running at bus speeds of up to 66MHz. The interposer board is an impedance controlled, matched trace length design that uses no active buffering. The analysis software for the logic analyzer provides clocking, setup and disassembly of PCI data.

NEX-PCIINTR Interposer

The NEX-PCIINTR interposer uses four Tektronix P6960 probes that are connected at right angles to the interposer. This reduces the keep-out volume required to use the interposer and allows the interposer to be used in systems with minimal clearance around the PCI cards. Please refer to the mechanical outline provided in this data sheet for details on the physical size of the NEX-PCIINTR interposer. Please call for information on a PCI interface adapter that is not an interposer.

NEX-PCIINTR Analysis Software

The included analysis software runs on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All PCI cycle types are identified. *Class*, *Sub-Class*, and *Prog. I/F* information is decoded to tell the user exactly what *Class* and *Sub-Class* of device is being accessed (mass storage, display, network, etc.). This information is also available in hexadecimal format. The command and status registers are also decoded and the bit-level information is displayed in an easy to read format. Invalid data bytes are dashed out during valid data cycles.

A major feature of the disassembly software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This allows the user to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and, using External clocking, acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

Fast 8GHz timing acquisition and low capacitive loading provide excellent timing analysis on every channel of the PCI bus.

Timestamp

All acquired data is time stamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this.

Correlation

While the NEX-PCIINTR5/3 package is being used with a Tektronix logic analyzer to monitor the PCI activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and PCI bus communication.

Setup/Hold Triggering

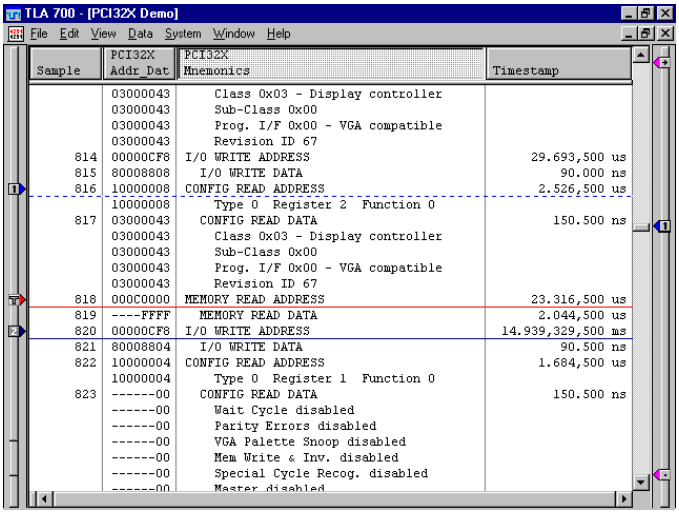
Setup and hold specifications can be verified, and margins tested, using the TLA700/7000 Logic Analyzer. Each channel group (address, data, control, etc.) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or any channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation. The timing resolution of the acquired data at the violation point is 8GHz (125ps).

Setup and hold margin testing can be done by altering the setup and hold times set for the violation trigger in 125ps increments. Changing these values until a violation occurs will show the actual setup and hold of the system under test.

Simultaneous State and Timing Acquisition

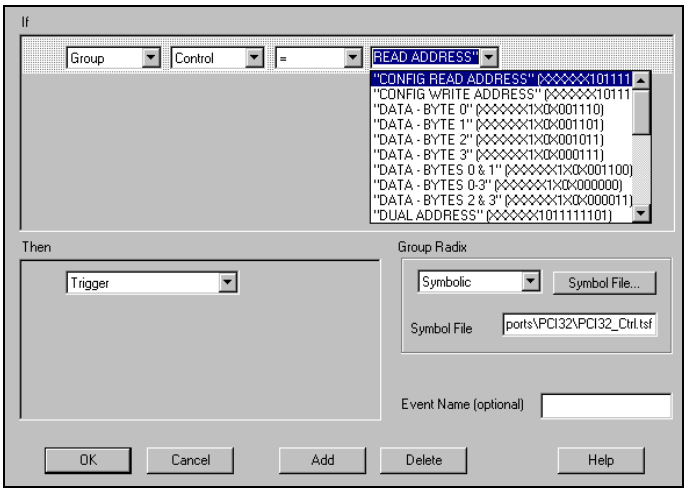
The Tektronix TLA700/7000 Logic Analyzer offers the unique capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-PCIINTR5/3 custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.

Disassembly (State Analysis)



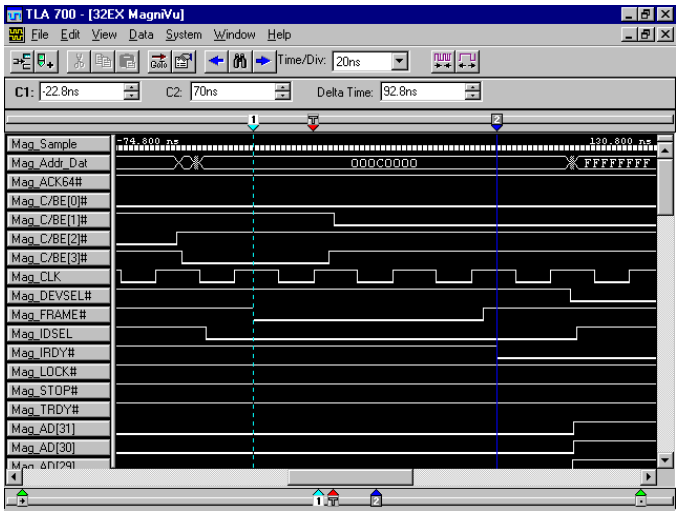
PCI cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class, and Type.

Triggering



Trigger on pre-defined PCI cycles

Timing Analysis

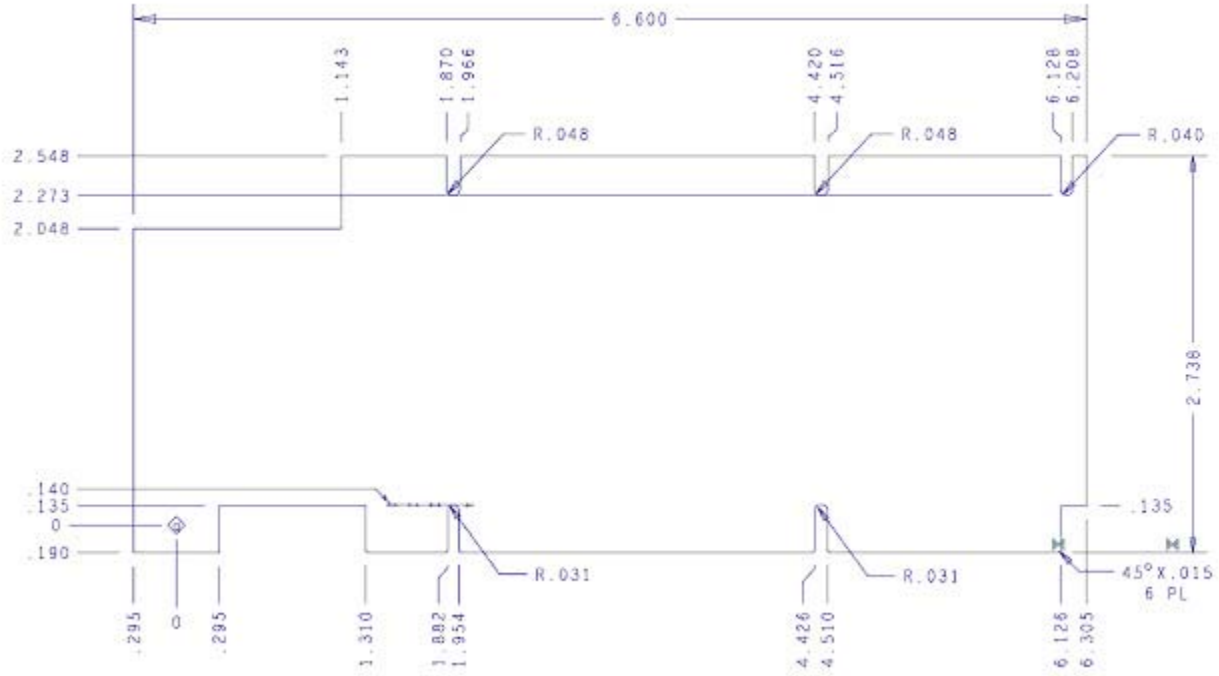


125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate PCI signal name. Bus format display of grouped signals shown.

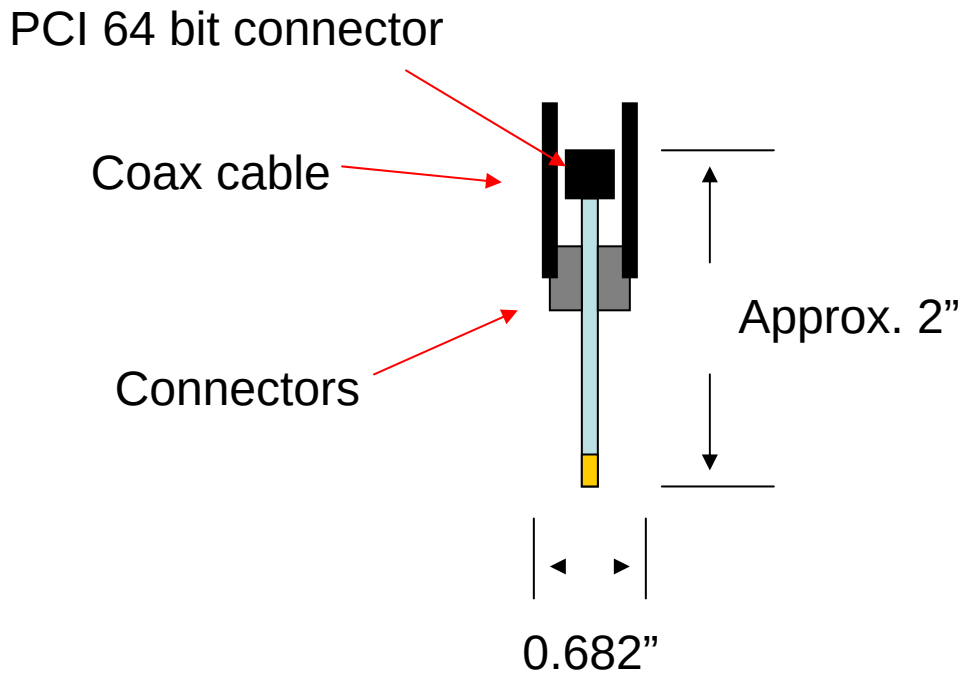
Tektronix Logic Analyzers Supported

PCI 3.3 or 5V
A Tektronix TLA700 or TLA7000 series Logic Analyzer with one 136-channel TLA7Ax4 acquisition module. Four P6960 probes are also required.

Mechanical Outline



Edge keep out with probes attached



Ordering / Contact Information

Part Number NEX-PCIINTR
Includes: PCI Bus Adapter
Software
Manual

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Nashua, NH 03062

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

