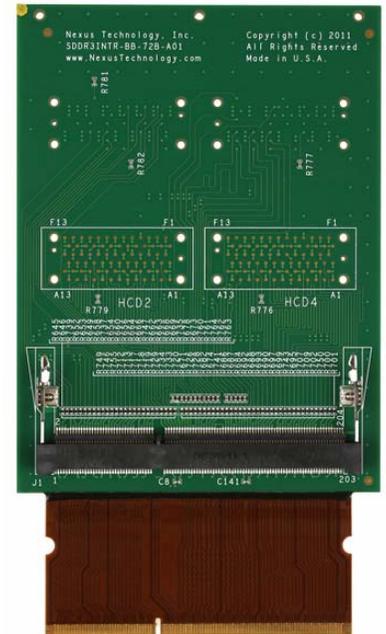


DDR3-1867 72-bit SODIMM Slot Interposer w/ECC

Flexible SODIMM Digital Validation



- High Speed DDR3 Digital Validation
- Passive 204-pin 72-bit SODIMM Slot Interposer
- Acquisition Up to DDR3-1867+
- Passive 50% Module Reduction w/MR Technology™
- Automated Logic Analyzer Setup
- DDR3 Protocol Violation Analysis
- Error Code Correction (ECC) Support
- Supports JEDEC EP3-6400, EP3-8500, EP3-10600, and EP3-12800 DDR3 modules
- Compatible with Nexus Memory Compliance Analyzer (MCA) Instrument



Passive Module Reduction (MR) Technology™

Nexus Technology's Module Reduction Technology™ is available with this interposer. Products implementing MR Technology™ allow for full acquisition, including read and write data, while cutting the hardware requirements in half.

Module Reduction Technology™ is a software solution. No qualifier sideband signals are required and no active circuitry is implemented in MR Technology™ which would otherwise force double-probing and increase the load on the DDR3 target.

Interposer Design

Nexus Technology recommends DDR3 slot interposers for applications where the customer must have the greatest flexibility in the probing of different 72-bit DDR3 SODIMMs.

This interposer is an extender design and does not require a dedicated SODIMM slot. The logic analyzer connects above the normal SODIMM height so that there is no mechanical interference with adjacent SODIMMs.

This is a passive interposer with no added buffers to conceal system performance.

Software

This DDR3-1867 72-bit SODIMM slot interposer comes with logic analyzer setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and protocol violation software.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions for easy display and logic analyzer triggering/filtering.

Data Sample Point Analysis Software



In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3 specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, make reliable and accurate DDR3 read and write data bus acquisition extremely difficult - if done manually. [NEX-DDR3-SPA](#), provided free, automates this process enabling quick and reliable DDR3 read and write data bus acquisition in only minutes. For more information, please see the [NEX-DDR3-SPA](#) product.

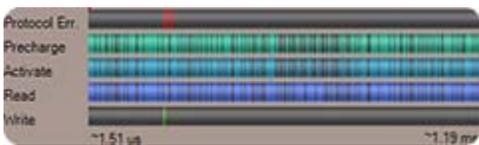
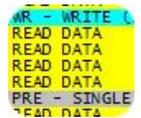
Protocol Violation Software



There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the [NEX-DDR-PROTOCOL](#) product for more information.

Digital Validation

Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the 800MHz command/address bus and acquires/reconstructs the 1,867MT/s read/write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.



These products also come with the [NEX-DDR-PROTOCOL](#) software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced protocol violation checking is available for purchase separately. Please see the [NEX-DDR-PROTOCOL](#) product for more information on this powerful tool.

Nexus Technology has designed this interposer to have a minimal effect in your target. As with any interposer solution, approximately one inch of trace length will be added between your target and the SODIMM. Depending on the target layout, memory controller, SODIMM type and SODIMM socket being probed, an interposer may affect the performance of your system. All users are given 30 days to qualify the interposer in their system. Should performance issues arise it is important to know that alternate solutions are available. Nexus Technology offers NEXVu SO-VDIMMs which provide both optimal probe points (at the memory components) and no added trace length or interposer effects. Also

available are memory component products which also provide optimal probe points, extremely small added trace lengths, and extremely small interposer effects.

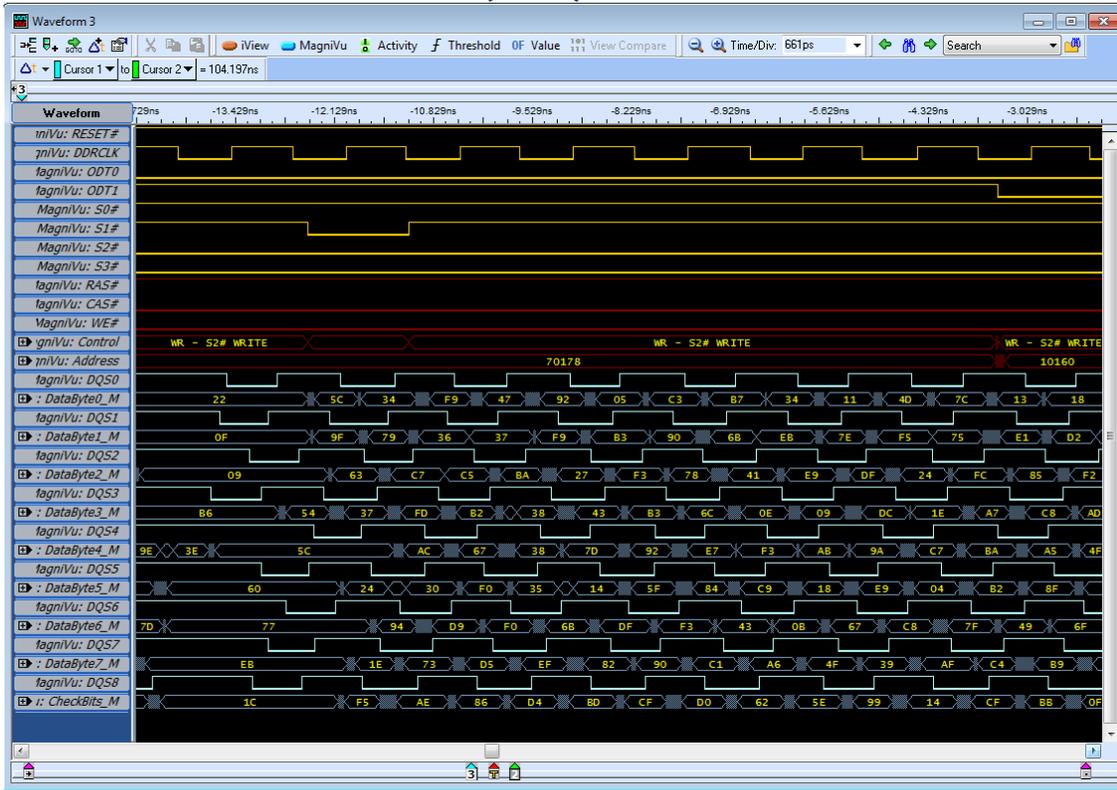
Performance You Can See™

The screenshot shows a software interface titled 'Listing 3' with a toolbar and a data table. The table has columns: Sample, Timestamp, R_SDDR3D_2C Mnemonics, R_SDDR3D_2C Address_0, R_SDDR3D_2C DataHi, R_SDDR3D_2C DataLo, and R_SDDR3D_2C ChkBits. The data rows show various memory operations like 'DESL - DEVICE DESELECT', 'WR - WRITE (S1#) Bank: 7', and 'WRITE DATA' with corresponding hexadecimal values and check bits.

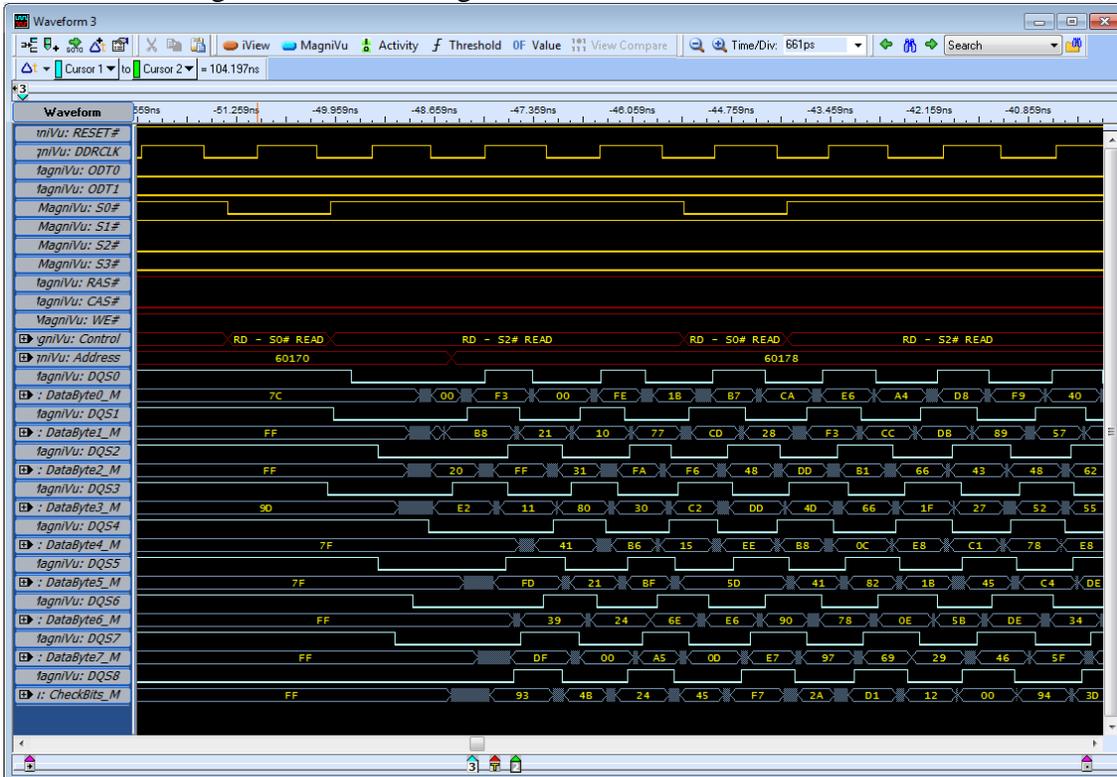
Sample	Timestamp	R_SDDR3D_2C Mnemonics	R_SDDR3D_2C Address_0	R_SDDR3D_2C DataHi	R_SDDR3D_2C DataLo	R_SDDR3D_2C ChkBits
487	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
488	2.383 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
489	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
490	2.363 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
491	625 ps	WR - WRITE (S1#) Bank: 7	70168	-----	-----	-----
492	2.363 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
493	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
494	2.403 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
495	625 ps	WR - WRITE (S1#) Bank: 7	70170	-----	-----	-----
496	2.363 ns	WRITE DATA	-----	EB77743E	B6091F22	9C
		WRITE DATA	-----	EB77605C	B6090F22	1C
497	625 ps	WRITE DATA	-----	EB77605C	B6090F22	1C
		WRITE DATA	-----	EE77605C	B6090F4C	1C
498	2.383 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
499	625 ps	WR - WRITE (S1#) Bank: 7	70178	-----	-----	-----
500	2.363 ns	WRITE DATA	-----	EF6B357D	B2BA3747	D4
		WRITE DATA	-----	82DF1492	3827F992	BD
501	625 ps	WRITE DATA	-----	90F35FE7	43F3B305	CF
		WRITE DATA	-----	C14384F3	B37890C3	D0
502	2.383 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
503	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
504	2.383 ns	WRITE DATA	-----	C449B2A5	1EFC757C	CF
		WRITE DATA	-----	B96F8F4F	A785E113	BB
505	625 ps	WRITE DATA	-----	07C1D01A	C8F2D218	0F
		WRITE DATA	-----	8593CA03	AD59CF2A	C4
506	2.343 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
507	625 ps	WR - WRITE (S0#) Bank: 1	10160	-----	-----	-----
508	2.403 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
509	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
510	2.363 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
511	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
512	2.363 ns	WRITE DATA	-----	3B6A201C	6768E9D4	AE
		WRITE DATA	-----	3B6A5D1C	6768FFD4	AE
513	625 ps	WRITE DATA	-----	3B6A5D1C	6768FFD4	AE
		WRITE DATA	-----	3E6A5D1C	6768FF9C	AE
514	2.403 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
515	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
516	2.363 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
517	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
518	2.383 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
519	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
520	2.363 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
521	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
522	2.383 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
523	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
524	2.363 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
525	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
526	2.383 ns	DESL - DEVICE DESELECT	-----	-----	-----	-----
527	625 ps	DESL - DEVICE DESELECT	-----	-----	-----	-----
528	2.383 ns	PDE - POWER DOWN ENTRY: CKE1 S3#	-----	-----	-----	-----

DDR3-1600 State Decode

Performance You Can See™ (cont.)



DDR3-1600 MagniVu Write Timing



DDR3-1600 MagniVu Reads Timing

Tektronix Hardware Requirements

DDR Speed	Acquisition	Mainframe Required	Module(s) Required	Probes Required**
DDR3>1333	Cmd/Address Read and Write	TLA7000	2- TLA7BB4 1.4GHz	1- Nexus NEX-PRB1XL 3- Tektronix P6960HCD
DDR3-1333	Cmd/Address Read and Write	TLA7000	1- TLA7BB4 750MHz (or 1.4GHz)	4- Nexus NEX-PRB1XL

**Please note that the NEX-SODDR3INTR72 requires 4- Tektronix P6960HCD probes at DDR3>1333.

Product Configuration Table

Nomenclature	Nexus Probes Included	Nexus Hardware Included	Nexus Software Included
NEX-SODDR3INTR72	No – Note 1	1- DDR3-1867 72-bit SODIMM Slot Interposer	1- TLA Setup & Protocol Decode Support Packages w/MR Technology™ 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation
NEX-SODDR3INTR72-PR1	Yes – Note 1	1- DDR3-1867 72-bit SODIMM Slot Interposer 1- NEX-PRB1XL	1- TLA Setup & Protocol Decode Support Packages w/MR Technology™ 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation
NEX-SODDR3INTR72-PR4	Yes – Note 2	1- DDR3-1867 72-bit SODIMM Slot Interposer 4- NEX-PRB1XL	1- TLA Setup & Protocol Decode Support Packages w/MR Technology™ 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation

Note 1: Four Nexus Technology NEX-PRB1XL probes can be used at/up to DDR3-1333 and can be ordered as a complete package as shown in the table above. One Nexus Technology NEX-PRB1XL and three Tektronix P6960HCD probes are required for DDR3>1333 (the P6960HCD probes must be purchased from Tektronix).

Note 2: Four Nexus Technology NEX-PRB1XL probes can be used at/up to DDR3-1333 and can be ordered as a complete package as shown in the table above. Four Tektronix P6960HCD probes are required for DDR3>1333 and must be purchased from Tektronix.

Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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