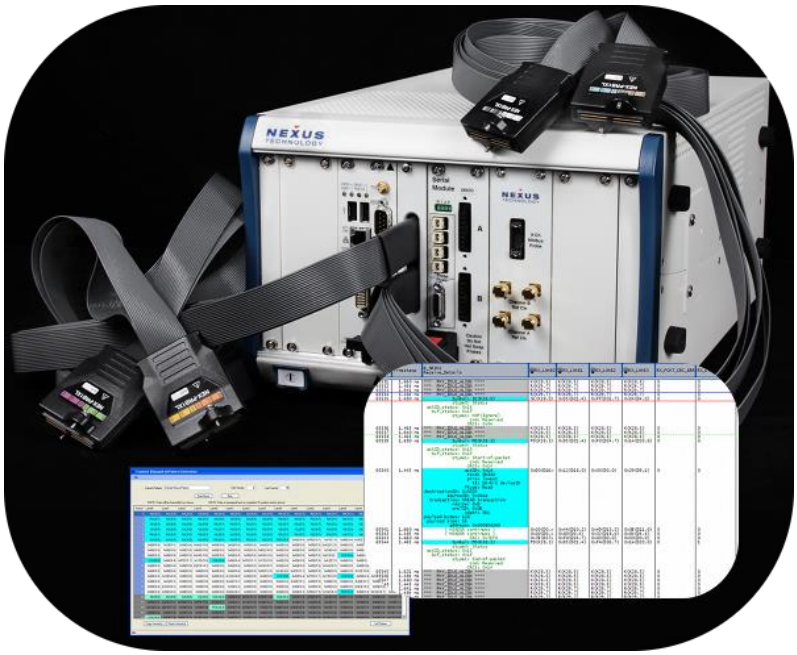
Serial RapidIO Gen2 Protocol Analyzer

Serial RapidIO Protocol Analyzer & Pattern Injector



- Supports Serial RapidIO Gen2 or Gen 1
- Descrambling & scrambling supported
- Tight integration and easy setup with award winning Tektronix analyzers
- x4, x2, and x1 serial widths (modes) supported
- 100% Capture
- All data rates supported from 6.25- to 1.25-Gbps
- Analyze two, one, or ½ links
- Analysis from PCS to full-duplex link exchanges (8b/10b to upper layer protocol (ULP)
- Real time analysis, filtering, and triggering
- Stimulus transmitter
- Pattern or error injection

This product enables passive monitoring, debugging, and complete target system analysis of all speeds of Serial RapidIO Gen2 and Gen1 from the physical coding-sublayer (PCS), through serial protocol, to full-duplex link protocol exchanges. Stimulus transmitters allow for stimulus injection of SRIO packets, control symbols, and 8b/10b characters.

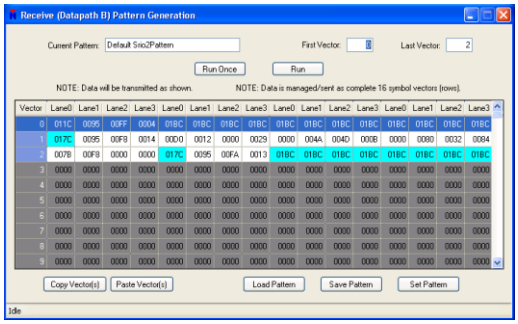
Capture / View / Expand

Tight integration with Tektronix equipment allows for simple setup and fast capture to quickly pinpoint and fix elusive problems. This integration also provides the widest possible expansion with pinpoint correlation on up to 48 independent buses simultaneously. Protect your investment with the industry's best and broadest test equipment for processor and bus support including FPGA verification, MIPI, DDR2, DDR3, and PCI Express.

- Automatic Descrambling
- Advanced and intuitive user experience
- Free offline software to share data with the whole team
- PCS Analysis
- Assistance in building custom control symbol or packet triggers
- Real time statistics
- Automatic decoding and display of lower and upper layer protocol

- Trigger / capture/ filter / view standard and custom packets
- Multi-level triggering across all channels
- Real-time filtering
- Predefined triggers for standard control symbols and packets
- Mark, search, and save acquired data
- 8b/10b. hex, and full decoding available in the same or separate displays
- TPI.NET API Library allows full control of the Tektronix test equipment using Microsoft's Visual Studio development platform.

Transmitter Traffic Generator



- x4, x2, or x1 lane widths supported
- Data rates of 6.25-, 5.00-, 3.125-, 2.50-, and 1.25-Gbps
- Import transmitter traffic from acquired data
- Physical Coding Sub Layer Features Supported
    - Transmitter generates the proper idle sequence (IDLE1 or IDLE2, if enabled) and transmits on each of the enabled lanes
    - Scrambles packet and control symbol data, if enabled
    - Injects lane stimulus (up to 64k-symbols) at proper time between idle sequences (IDLE1 or IDLE2, if enabled)
    - Transmitter can also loop indefinitely on an 64k-symbol pattern
    - Transmits 10b symbols and maintains running disparity to specification

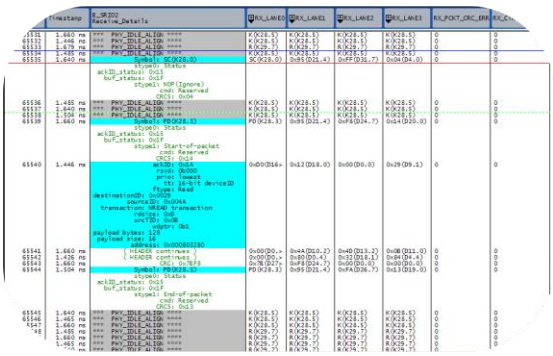
Product Details

Acquisition of Serial RapidIO x4/x2/x1, full-duplex mode links is available for all speeds of Serial RapidIO up to 6.25-Gbps. The Serial RapidIO data is automatically descrambled, decoded and aligned, for easy debug and analysis. Real-time error checking capabilities allow the user to quickly root-cause system level failures.

Real time filtering can be used to filter out IDLE sequences and other types of data to more efficiently capture and store the packet and control symbol data. This allows the user to capture an event of interest as well as the conditions that resulted in the occurrence of that event on the Serial RapidIO bus.

This product also supports transmission of stimulus data, including SRIO packets, control symbols and 8b/10b characters in x4/x2/x1 mode. These transmitters allow testing of Serial RapidIO receivers on a user system for different link conditions and error recovery logic. The transmitters can also be used as a substitute for the Serial RapidIO transmitter on the user system to quickly recreate infrequent events and test the system response. Stimulus data can be injected into a continuous IDLE sequence or the stimulus can loop on a predefined data pattern. 64k-Symbols of stimulus memory is available.

Protocol Analysis Features



- Embedded clock recovery
- x4, x2, or x1 lane widths supported
- Data rates of 6.25-, 5.00-, 3.125-, 2.50-, and 1.25-Gbps
- Physical Coding Sub Layer Features Supported
    - 8b/10b decoding
    - Flexible synchronization state machine
    - Flexible alignment state machine
    - Marking of invalid code groups
    - Automatic descrambling of packet and control symbol data as required
- All packets and all packet fields from LP-Serial physical layer, PCS, and PMA layers available for analysis
- Long and short control symbol formats supported
- Real-time CRC checking for packets and long/short control symbols (CRC-16, CRC-13, & CRC-5)
- Visibility and storage of the acquired and analyzed data is provided through a Tektronix logic analyzer

The product supports the real time monitoring and triggering of a full duplex link for the following conditions.

Real time filtering and triggering on full packets and control symbols is also available.

CRC Error (Control Symbol or Packet)
Disparity Error – Each Lane
Lanes Locked to Data
Lanes Synchronized
Lanes Aligned
Invalid Character in Symbol or Packet
Idle
Packet Header
SC Control Symbol
PD Control Symbol
PD SOP Control Symbol
PD Cancel Control Symbol
PD EOP Control Symbol

Figure 1 Real Time Analysis Features

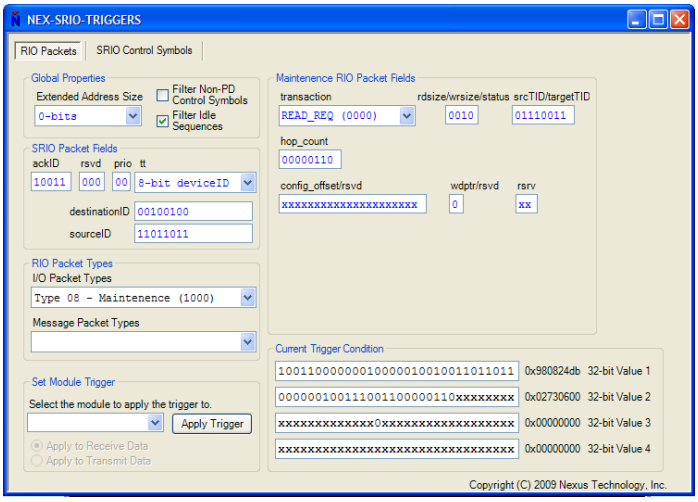
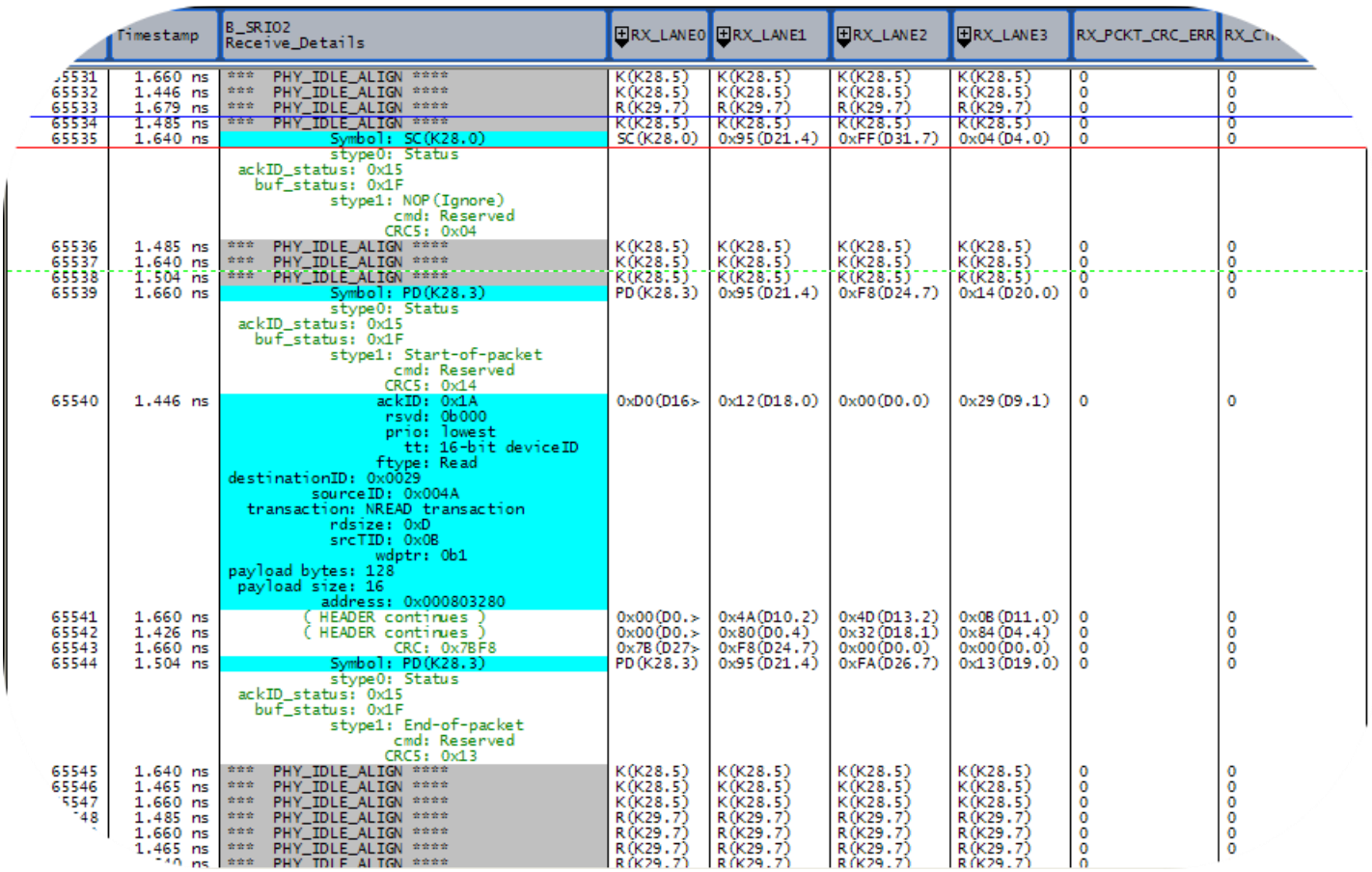


Figure 2 Real Time Packet Triggering / Filtering



	Timestamp	B_SRIO2 Receive_Details	RX_LANE0	RX_LANE1	RX_LANE2	RX_LANE3	RX_PCKT_CRC_ERR	RX_CH...
65531	1.660 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65532	1.446 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65533	1.679 ns	*** PHY_IDLE_ALIGN ****	R(K29.7)	R(K29.7)	R(K29.7)	R(K29.7)	0	0
65534	1.485 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65535	1.640 ns	Symbol: SC(K28.0) stype0: Status ackID_status: 0x15 buf_status: 0x1F stype1: NOP(Ignore) cmd: Reserved CRC5: 0x04	SC(K28.0)	0x95(D21.4)	0xFF(D31.7)	0x04(D4.0)	0	0
65536	1.485 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65537	1.640 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65538	1.504 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65539	1.660 ns	Symbol: PD(K28.3) stype0: Status ackID_status: 0x15 buf_status: 0x1F stype1: Start-of-packet cmd: Reserved CRC5: 0x14	PD(K28.3)	0x95(D21.4)	0xF8(D24.7)	0x14(D20.0)	0	0
65540	1.446 ns	ackID: 0x1A rsvd: 0b000 prio: lowest tt: 16-bit deviceID ftype: Read destinationID: 0x0029 sourceID: 0x004A transaction: NREAD transaction rdsize: 0xD srcTID: 0x0B wdptr: 0b1 payload bytes: 128 payload size: 16 address: 0x000803280	0xD0(D16>	0x12(D18.0)	0x00(D0.0)	0x29(D9.1)	0	0
65541	1.660 ns	(HEADER continues)	0x00(D0.>	0x4A(D10.2)	0x4D(D13.2)	0x0B(D11.0)	0	0
65542	1.426 ns	(HEADER continues)	0x00(D0.>	0x80(D0.4)	0x32(D18.1)	0x84(D4.4)	0	0
65543	1.660 ns	CRC: 0x7BF8	0x7B(D27>	0xF8(D24.7)	0x00(D0.0)	0x00(D0.0)	0	0
65544	1.504 ns	Symbol: PD(K28.3) stype0: Status ackID_status: 0x15 buf_status: 0x1F stype1: End-of-packet cmd: Reserved CRC5: 0x13	PD(K28.3)	0x95(D21.4)	0xFA(D26.7)	0x13(D19.0)	0	0
65545	1.640 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
65546	1.465 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
5547	1.660 ns	*** PHY_IDLE_ALIGN ****	K(K28.5)	K(K28.5)	K(K28.5)	K(K28.5)	0	0
548	1.485 ns	*** PHY_IDLE_ALIGN ****	R(K29.7)	R(K29.7)	R(K29.7)	R(K29.7)	0	0
	1.660 ns	*** PHY_IDLE_ALIGN ****	R(K29.7)	R(K29.7)	R(K29.7)	R(K29.7)	0	0
	1.465 ns	*** PHY_IDLE_ALIGN ****	R(K29.7)	R(K29.7)	R(K29.7)	R(K29.7)	0	0
	ns	*** PHY_IDLE_ALIGN ****	R(K29.7)	R(K29.7)	R(K29.7)	R(K29.7)	0	

Figure 3 6.25Gbps, 4x Mode Protocol Analysis Example Display

Bus Configuration & Stimulus Control Interface

The configuration of the SRIO bus receivers and transmitters are available through a simple user interface.

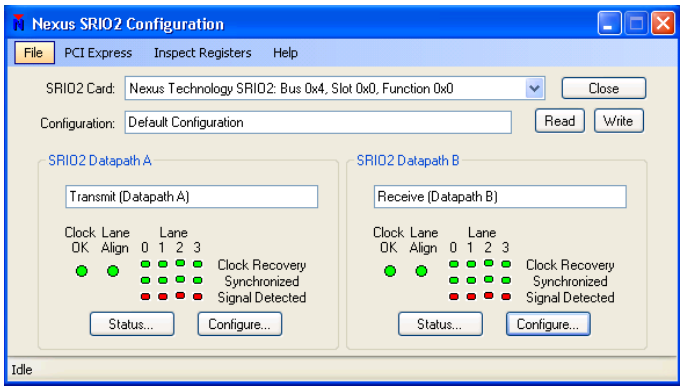


Figure 4 Main Configuration Interface

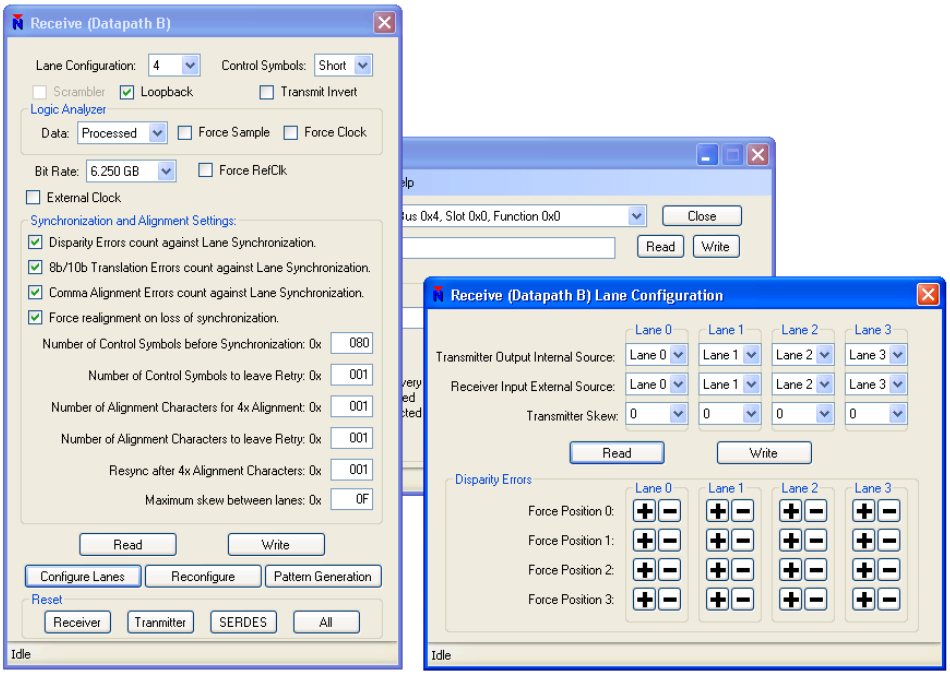


Figure 5 Configuration Interface Details

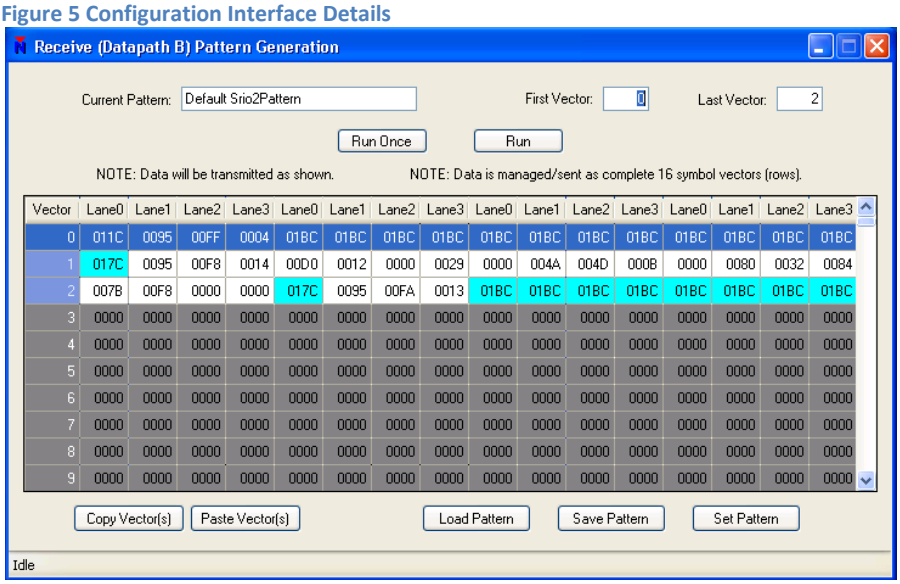


Figure 6 Pattern Injector Configuration Interface

Connection to Target

Two target connections are available through the use of Nexus Technology single channel serial probes or a midbus probe. These probes have similar electrical but very different mechanical specifications.

Data eyes presented to the probe must meet or exceed the minimum eyes requirements for reliable capture of SRIO traffic. Load models are available for verification of eye size at the probe point. Please contact us for information on these models. The eye size is measured from the point of probing as the width and height of the eye that forms a diamond shape.

The minimum specified eye sizes may only be available at specific distances from the drivers of the signals. If the target was designed and tuned correctly, the eye size should be most open very close to the receiver of the signals. For these reasons, it is recommended that the probe points be as close to the receiver as possible. The receiver capacitors make very good connection points for the single channel serial probe.

Minimum Eye Height (single ended)	30mV
Minimum Eye Width @ 6.25Gb/s	90ps
Minimum Eye Width @ 5.00Gb/s	110ps
Minimum Eye Width @ 3.125Gb/s	180ps
Minimum Eye Width @ 2.50Gb/s	220ps
Minimum Eye Width @ 1.25Gb/s	430ps

Table 1Minimum Eye Sizes at Probe Point

6.25-Gbps Midbus Probe

For targets with 8ch midbus probe footprints, the customer can use the NEX-PRB8-SM serial midbus probe. This probe provides easy access with minimal interference. Pin swapping is allowed inside of the TX (blue below) or RX (green below) signals only. Swapping between the TX and RX signals is not allowed.

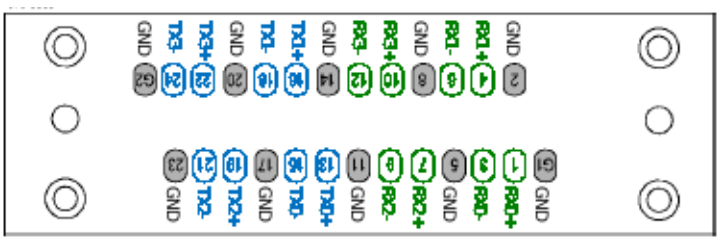


Figure 7 NEX-PRB8-SM 8ch Midbus Pin Assignments

Pin #	Signal	Tek. Lane #	Pin #	Signal	Tek. Lane #	Alt. Datapath Name
2	GND		**1**	RD0+	0	Datapath B
4	RD1+	1	**3**	RD0-	0	
6	RD1-	1	**5**	GND		
8	GND		**7**	RD2+	2	
10	RD3+	3	**9**	RD2-	2	
12	RD3-	3	**11**	GND		
14	GND		**13**	TX0+	4	Datapath A
16	TX1+	5	**15**	TX0-	4	
18	TX1-	5	**17**	GND		
20	GND		**19**	TX2+	6	
22	TX3+	7	**21**	TX2-	6	
24	TX3-	7	**23**	GND		

Table 2 NEX-PRB8-SM 8ch Midbus Pin Assignments

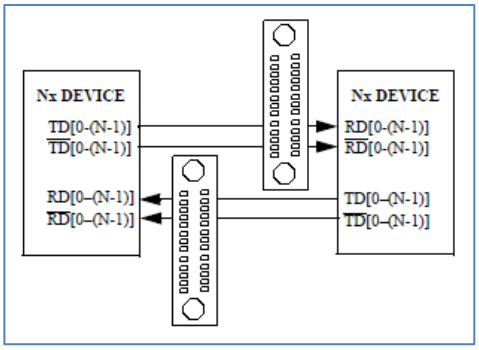


Figure 8 Recommended Midbus Probing

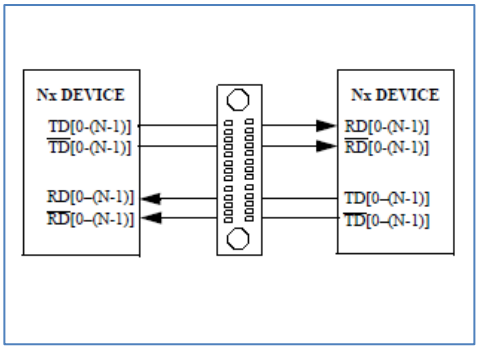


Figure 9 True Midbus Probing

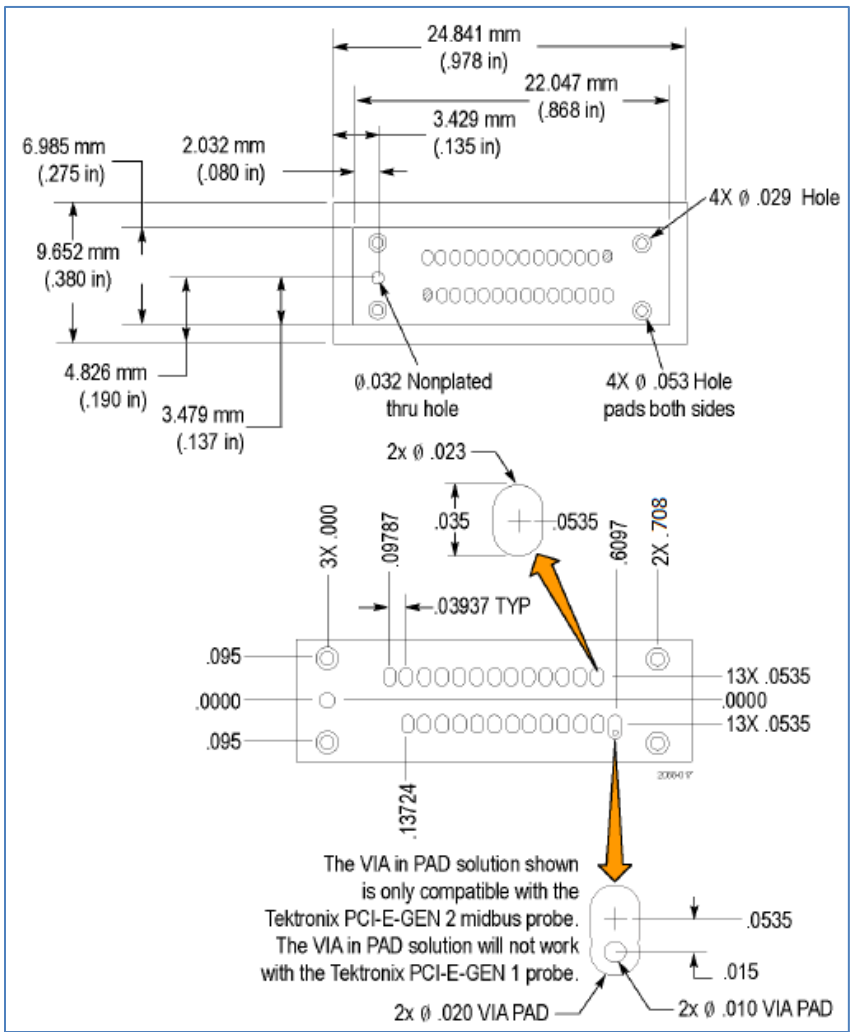


Figure 10 NEX-PRB8-SM Probe Footprint Dimensions and Keep Out Area

6.25-Gbps Single Channel Probe

For targets without midbus probe footprints, the customer can use NEX-PRB1-SD probe(s). These probes connect directly to the target board at any conductive point in the circuit.

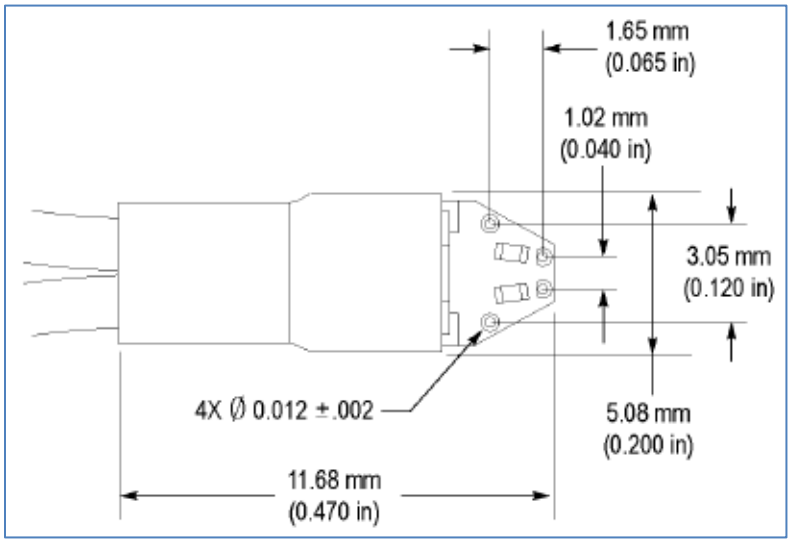


Figure 11 NEX-PRB1-SD Single Channel Serial Probe Dimensions

Serial RapidIO Gen2 Protocol Analyzer

NEX-SRIO2 Technical Specification

General

Specification	Detail
Interface Type	Active Serial Preprocessor
LA Interface	Direct attach to Tektronix logic analyzer module(s)
Target Interface	NEX-PRB8-SM or NEX-PRB1-SD serial probe(s)
RapidIO Specifications Supported	2.1 and 1.3
Serial RapidIO Modes Supported	1x, 2x, and 4x
Serial RapidIO Bit Rates Supported (Gb/s)	6.25-, 5.00-, 3.125-, 2.50-, and 1.25-
Min. Eye Height (Single Ended)	30mV
Min. Eye Width (@ 6.25Gb/s)	90ps

Tektronix Recommended Hardware Requirements General

Specification	Detail	Quantity
Logic Analyzer Mainframe	TLA7000 or TLA6000 Series	1
Logic Analyzer Module(s)	Varies	Varies
Logic Analyzer Probes	None needed.	

Product Configurations

Multi-bus configurations are available for two or more full duplex acquisition. Please contact us for more information.

The following single bus (full-duplex) configurations are:

Nomenclature	Data Rates (Gbps)	Links Supported	Injection Transmitters	Descrambling / Scrambling
NEX-SRIO2-1	3.125, 2.50, 1.25	1- Full Duplex	0	No
NEX-SRIO2-1-T	3.125, 2.50, 1.25	1- Full Duplex	1	No
NEX-SRIO2	6.25, 5.0, 3.125, 2.50, 1.25	1- Full Duplex	0	Yes
NEX-SRIO2-T	6.25, 5.0, 3.125, 2.50, 1.25	1- Full Duplex	1	Yes

Table 3 Base Product Configurations

Upgrade Nomenclature	Prerequisite	Data Rates (Gbps)	Links Supported	Injection Transmitters	Descrambling / Scrambling	Notes
NEX-SRIO2-U2	NEX-SRIO2-1(-T)	6.25, 5.0, 3.125, 2.50, 1.25	1- Full Duplex	Dependent on 'T' option in prereq.	Yes	Upgrade to max. of 6.25Gbps
NEX-SRIO2-U1T	NEX-SRIO2-1	3.125, 2.50, 1.25	1- Full Duplex	1	No	Add transmitter to 3.125Gbps
NEX-SRIO2-U2T	NEX-SRIO2	6.25, 5.0, 3.125, 2.50, 1.25	1- Full Duplex	1	Yes	Add transmitter to 6.25Gbps

Table 4 Nomenclature Configurations for Future Add Ons (differences highlighted in yellow)

Tektronix Recommended Equipment

Nomenclature	Recommended Tektronix Equipment (Full Duplex)	Recommended Tektronix Equipment (1/2 Duplex)	Notes
NEX-SRIO2-1(-T)	1- TLA6204 Opt. 45	1- TLA6202 Opt. 45	No upgrade paths for the Tektronix equipment. Recommend NEX-SRIO2(-T) (see below) equipment if future upgradability is desired.
NEX-SRIO2(-T)	1- TLA7000 & 1-TLA7BB4	1- TLA7000 & 1-TLA7BB2	Future upgrade from ½ duplex to full duplex would require a second TLA7BB2 module.

This product supports the entire TLA6000 and TLA7000 series logic analyzer modules, including the TLA7ACx and TLA7BBx family of modules. For a complete list of supported SRIO2 configurations and Tektronix hardware, please contact us.

Product Support

Product Support is critical to your success. Our engineering staff can provide expert training and support tailored to your specific needs. Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

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